

LESSON 5 – ULTRA-LOW POWER AND EFFICIENT ELECTRONICS

Franco Maloberti

Franco Maloberti

- 1968 – Laurea degree in Physics (University of Parma)
 - 1993– Visiting Professor ETH Zurich
 - 1996 – Honorary PhD (INAOE Mexico)
 - 1968 – 2000 – Assistant/Associate/full Professor, University of Pavia
 - 2000 – 2002 – J. Kilby Chair Professor Texas A&M University
 - 2002 – 2004 – Microelectronics Chair Professor UT Dallas
 - 2004 – Visiting Professor EPFL
 - 2004 – 2016 – Professor, University of Pavia
 - 2012 – Chair Academic Committee SKL University of Macau
 - 2016 - Emeritus Professor, University of Pavia
 - 2022 - Division I Director IEEE
 - 2024 - Honorary PhD (University Macau – China SAR)
-
- Interests: analog IC, data converters, ultra-low-power, power management, sensor interfaces



LESSON 5 – ULTRA-LOW POWER AND EFFICIENT ELECTRONICS

Franco Maloberti

1. Introduction – topics covered, general overview
2. Voltage management – generate supply voltage for EAWS
3. Energy storage management – charge regulation circuits
4. Sensor electronics
5. Analog to Digital Conversion
6. Low Voltage Low Power Circuits

1. Introduction – topics covered, specifications

Course contents

Objectives:

- To provide the essential knowledge for understanding circuit operation
- To give an overview of the existing approaches, either academic or commercial
- To provide guidelines in selecting components and dimensioning circuits

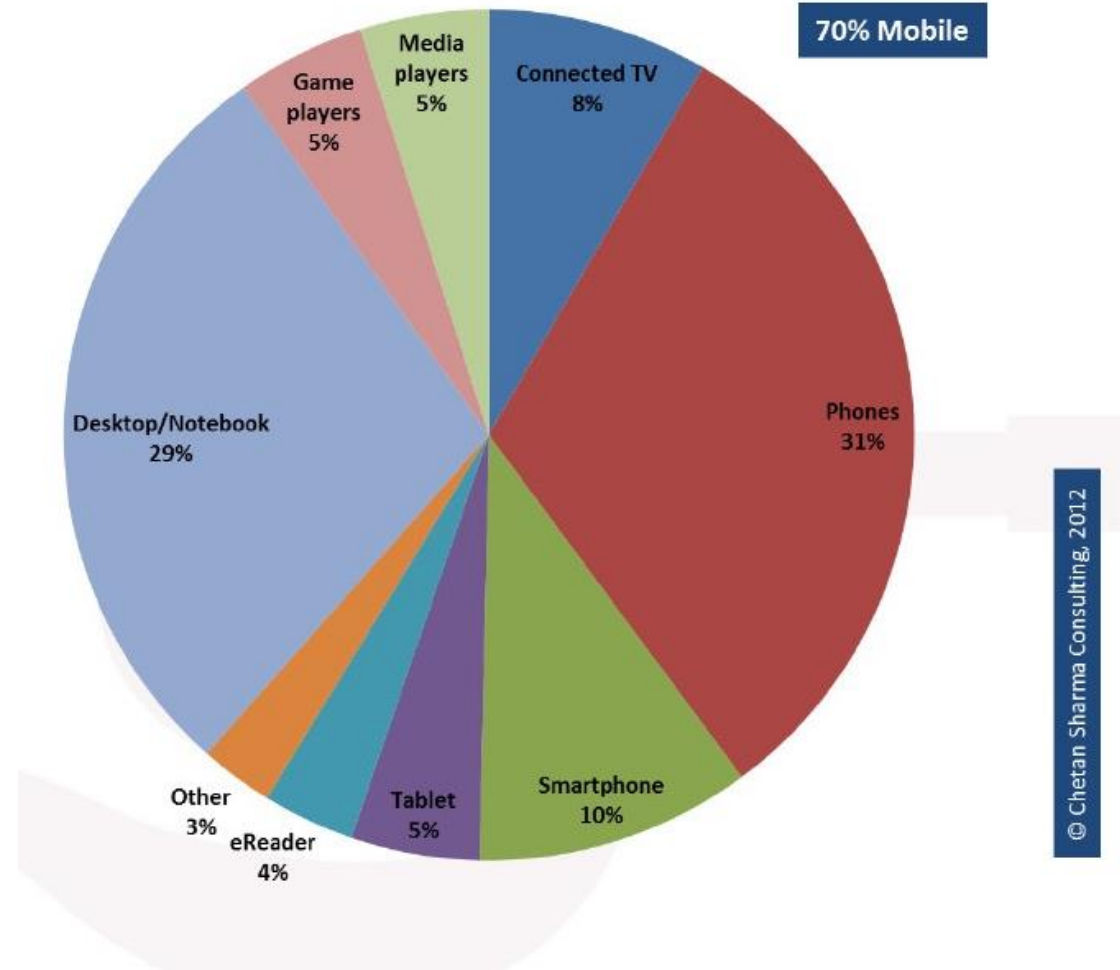
For the following circuits found in energy autonomous systems :

- Voltage conversion from transducer levels to system voltage
- Startup circuits and strategies
- Energy storage circuits
- Sensor front-end electronics
- Analog to Digital conversion

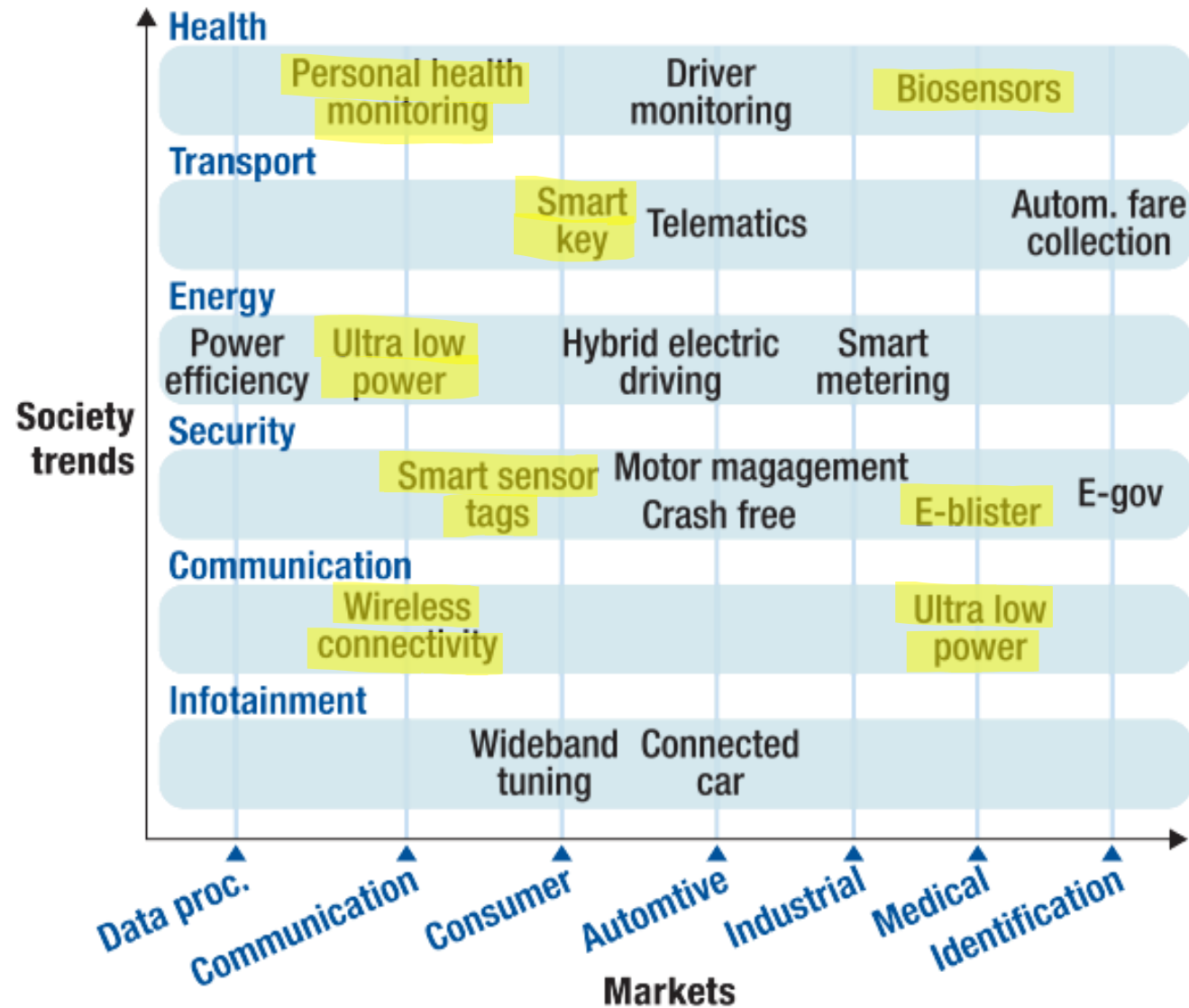
1.1 Autonomous Wireless Systems

MODERN SYSTEMS

- Key features
 - Wired
 - Mobile
- What about Power?
 - Refueled
 - Autonomous

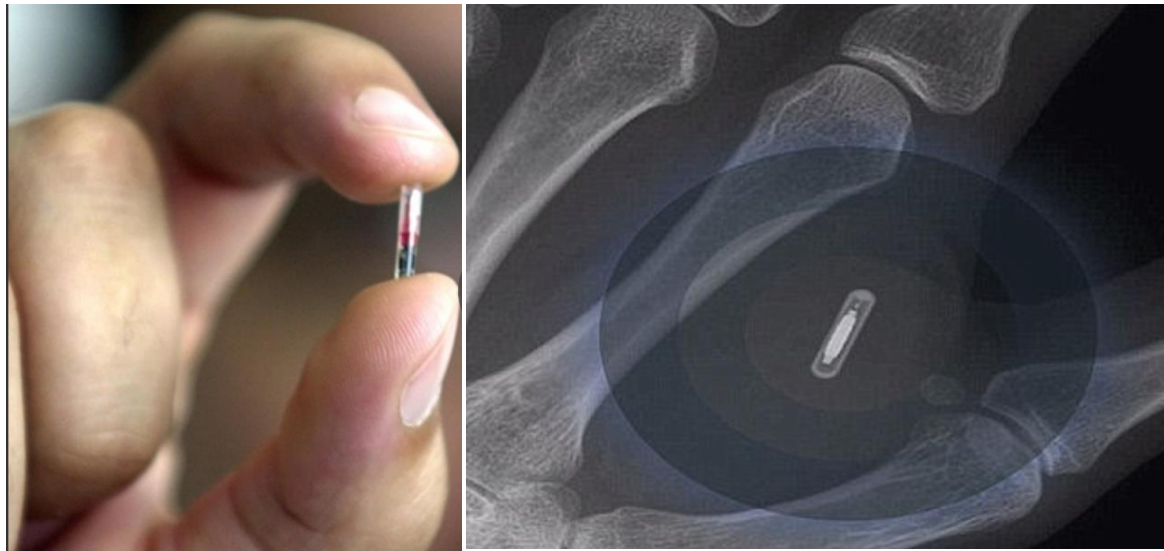
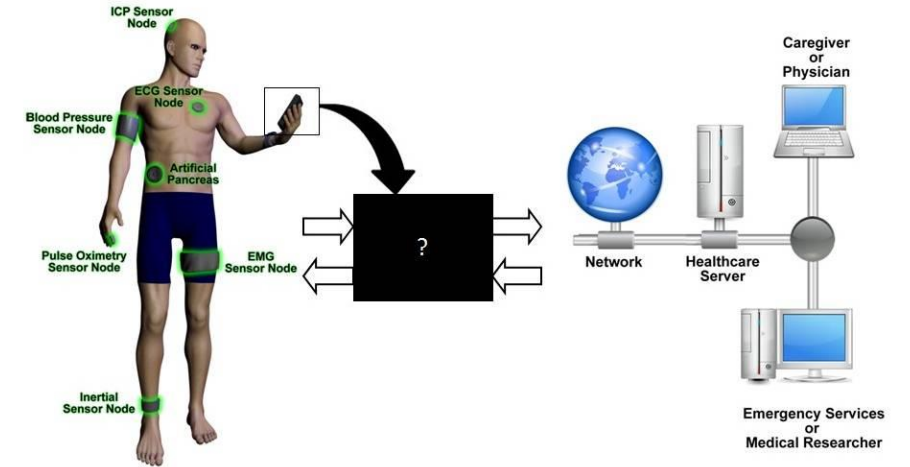
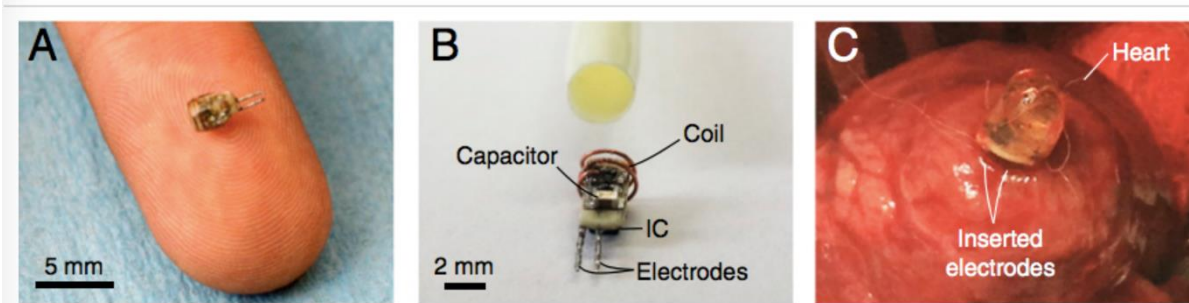


1.1 Autonomous Wireless Systems



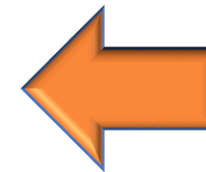
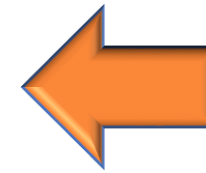
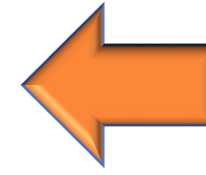
1.1 Autonomous Wireless Systems

VARIOUS APPLICATIONS



1.1 Autonomous Wireless Systems

- ◆ Sensors
- ◆ Analog processing and data conversion
- ◆ Low power and short range communication



1.1 Autonomous Wireless Systems

Microelectronics and quality of life

Textile sensors



**Textiles capable to measure
Bio-mecanical and physiological signals**

- ◆ Smart materials embedded into fibers
- ◆ For multi-parameter analysis

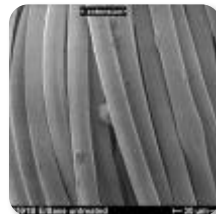
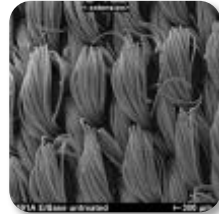
1.1 Autonomous Wireless Systems

Textile for sensors

Research in material science

Electrical properties

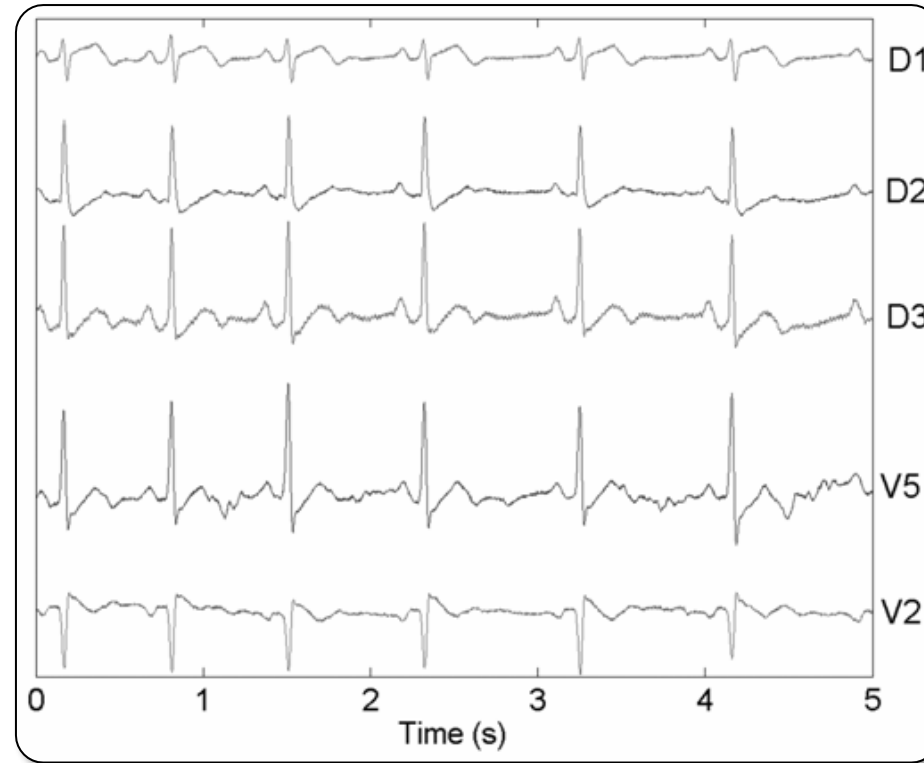
- Metallic wires
- Conductive coating



Bekinox® VS is a sliver of 100 % stainless steel fibres.

1.1 Autonomous Wireless Systems

ECG



5 signals at the same time

- ▶ Einthoven Leads: D1, D2, D3
- ▶ Precordial Leads: V2, V5

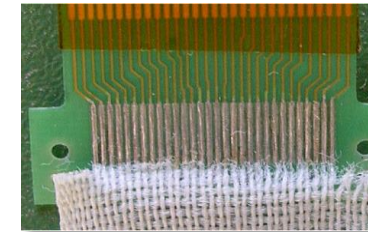
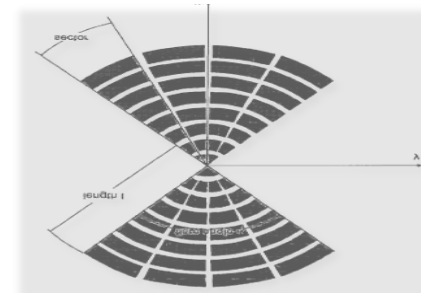
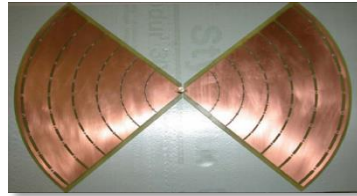
1.1 Autonomous Wireless Systems

Safety

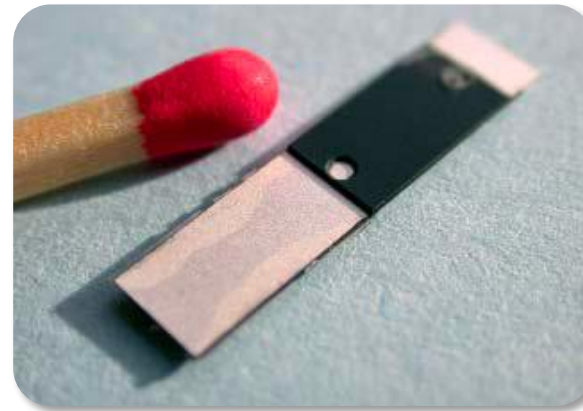
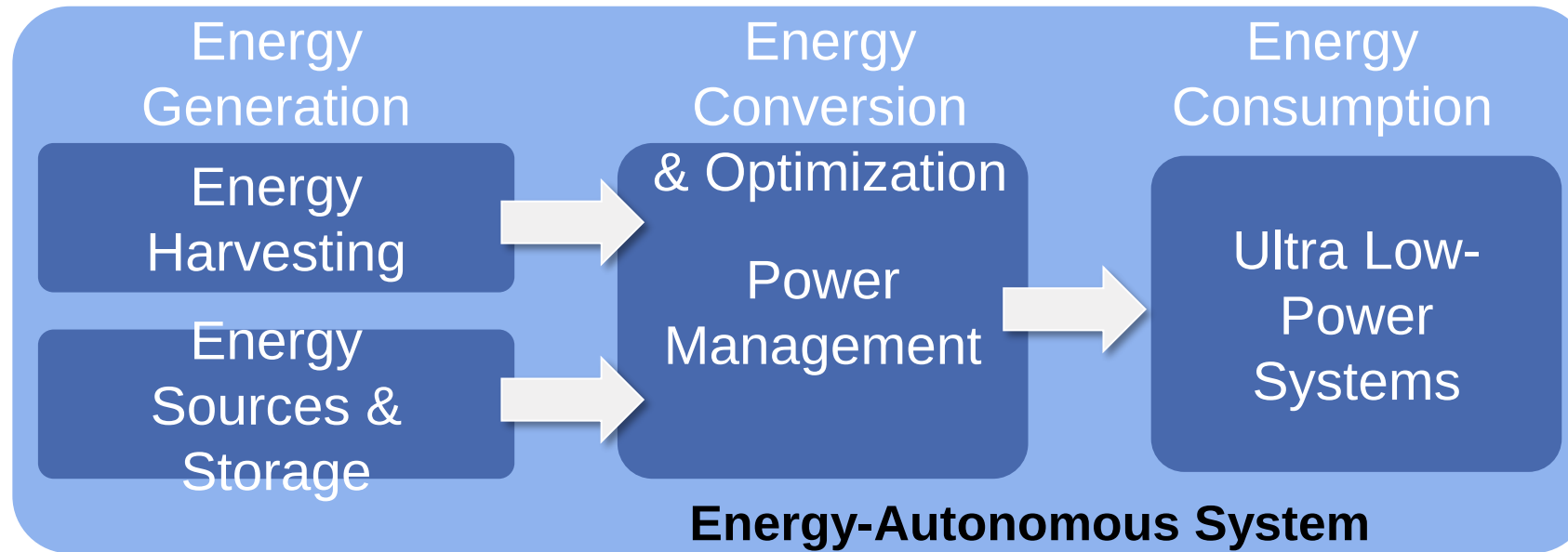


BSPP/R.DOSNES

Antennas for communication

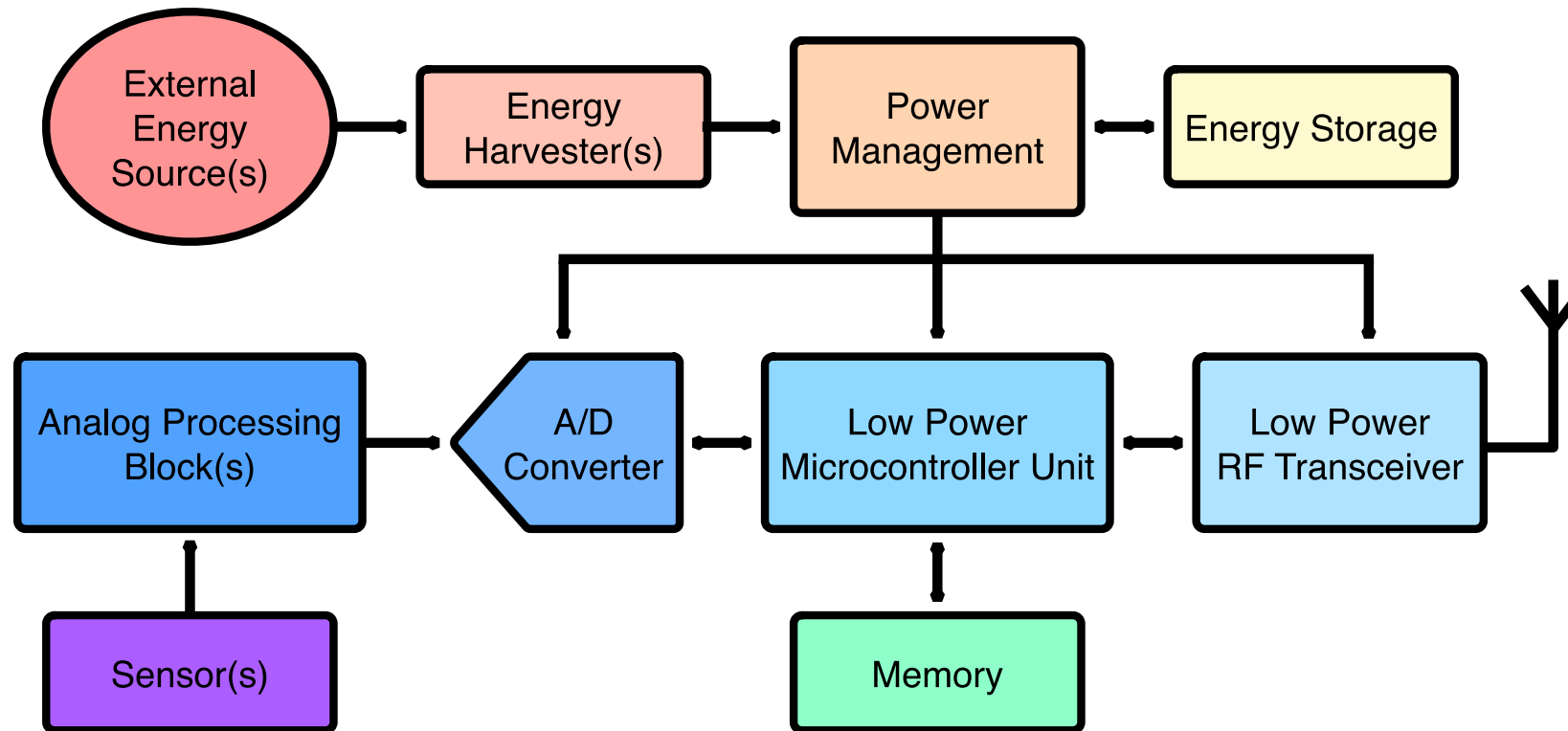


1.1 Autonomous Wireless Systems



1.1 Autonomous Wireless Systems

- More and more used in the future are the systems that do not need and/or do not have the possibility of refueling power.



1.1 Autonomous Wireless Systems

WHAT IS CRITICAL?

COMMUNICATION

Range of operation, protocols, ...

POWER

Refueling or Harvesting power. Storing Power Optimal use of Power

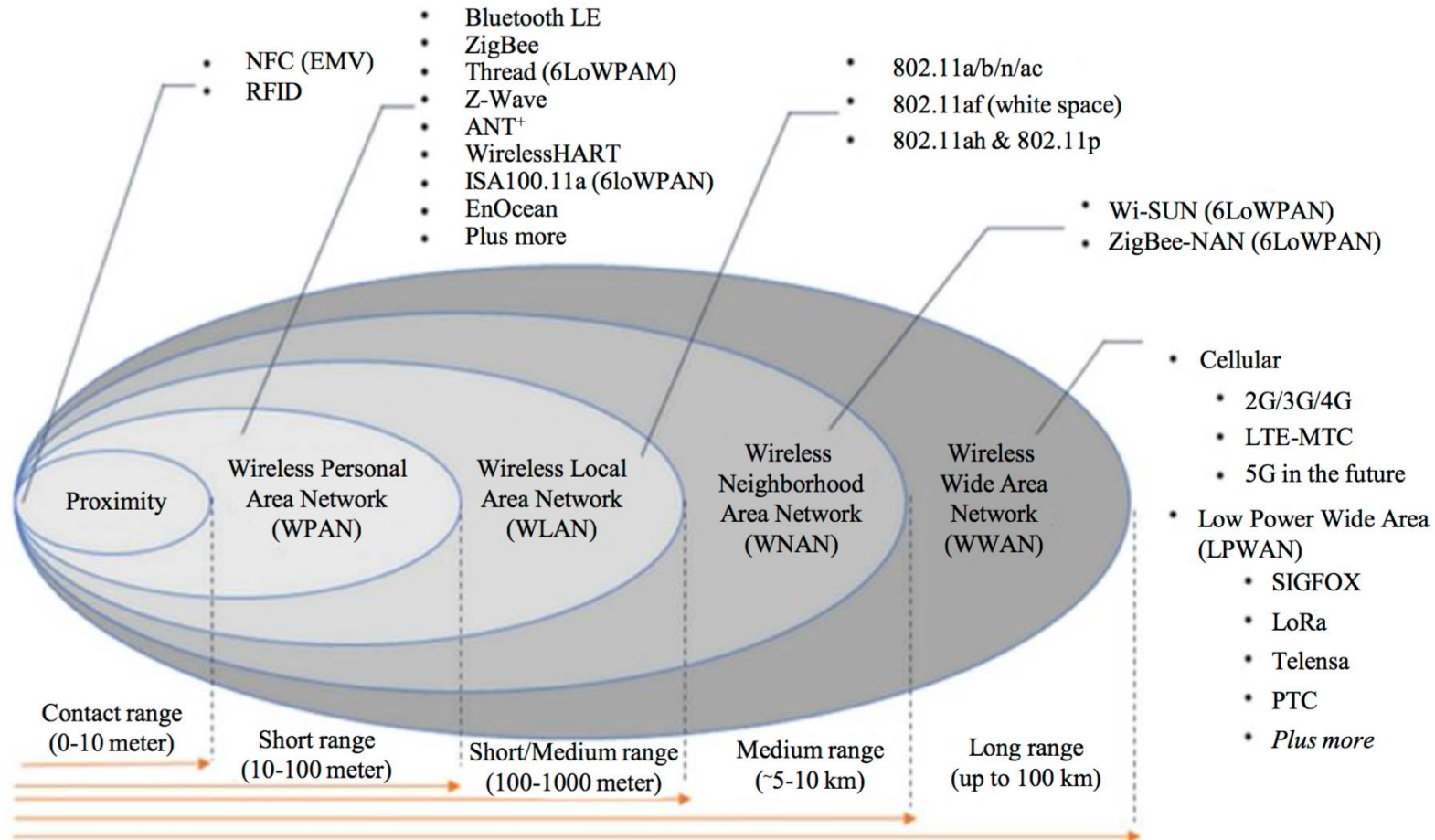
SENSING AND SIGNAL PROCESSING

Miniaturized sensors, Analog/digital system partitioning,
Voltage of operation, Nanopower circuits



1.1 Autonomous Wireless Systems

- What is the expected communication range?



1.1 Autonomous Wireless Systems

- For short to medium range communication Wireless Personal and Local Area Network technologies (WPAN\LAN) such as: Bluetooth, ZigBee, 6LowPAN, and Wi-Fi are used.

Table 1. Particular comparison for different low power Wi-Fi modules.

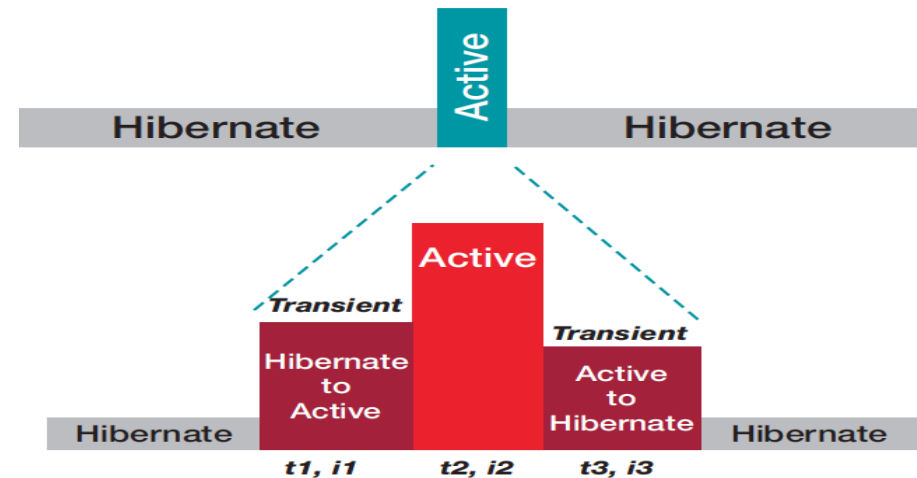
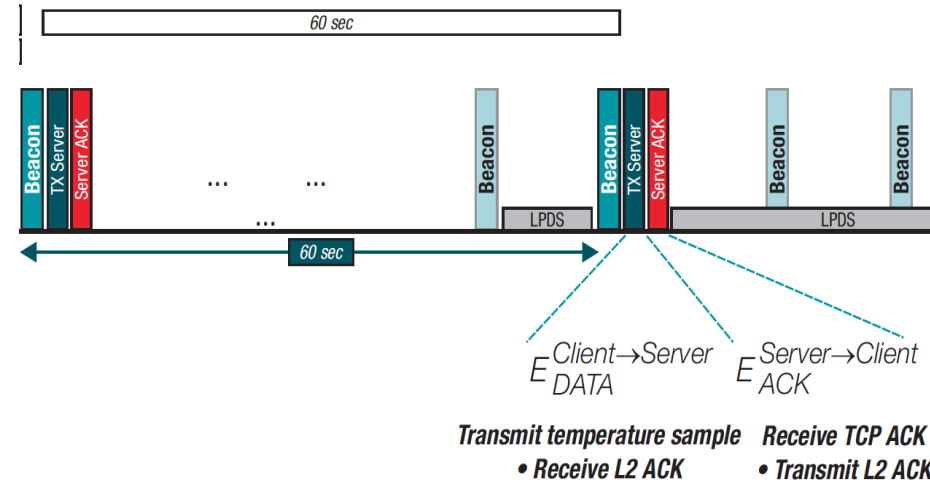
Company	Module	IEEE Protocol	V _{DD} (Volt)	I _{TX} (mA)	I _{Rx} (mA)	I _{sleep} (μA)	Max. Bit Rate (Mb/S)
Microchip [9]	RN171	802.11 b/g	3.3	190	40	4	54
Qual Comm [13]	QCA4004	802.11 n	3.3	250	75	130	10
Gain Span [14]	GS1011M	802.11 b	3.3	150	40	150	11
G2 Microsystem [15]	G2M5477	802.11 b/g	3.3	212	37.8	4	11
Redpine [16]	RS9110-N-11-02	802.11 b/g/n	3.3	19	17	520	11
RTX [17]	RTX41x Series	802.11 b/g/n	3.3	0.760	0.760	3	10

- Power lower by a factor 10 for dedicated modules.
- Very low duty cycle and very low current in the sleep mode.

1.1 Autonomous Wireless Systems

Example: temperature sensor,
transmits data every 60 s.
Power in the sleep mode
dominant

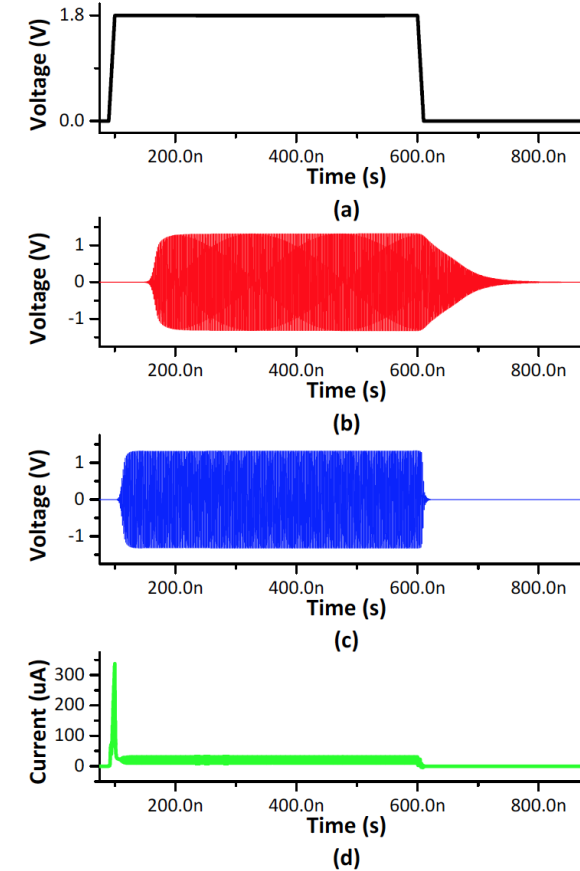
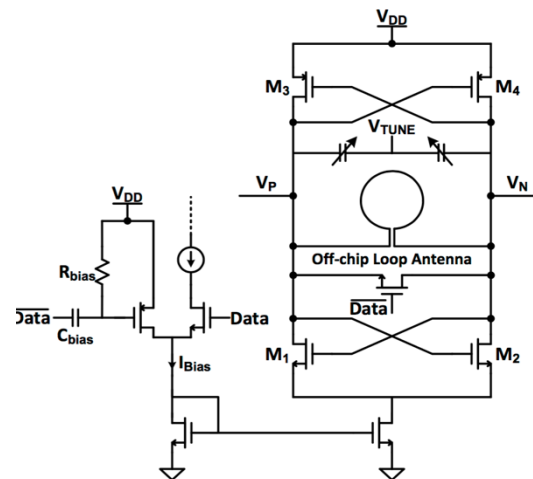
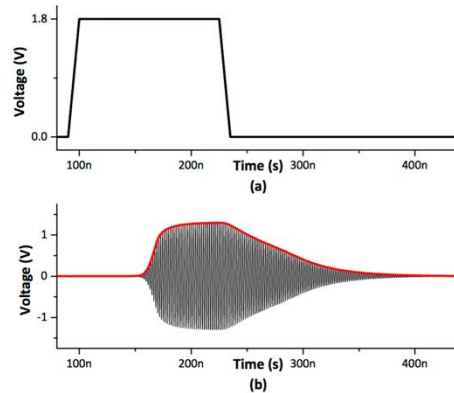
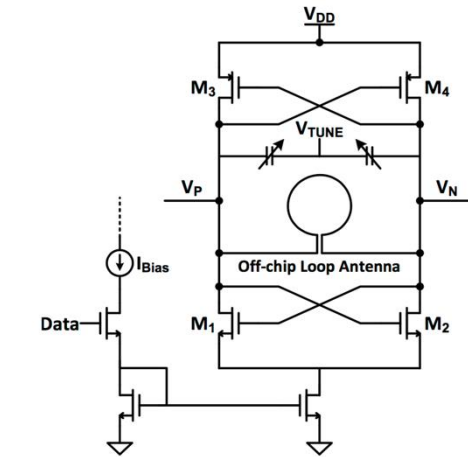
Consumes power for waking-
up and sending to sleep.
How to wakeup and to
hibernate in negligible time?



1.1 Autonomous Wireless Systems

FAST WAKE-UP

Simple solution
for OOK Medical
Transmitter



Ture, Kilnic, Maloberti, Dehollain : ISCAS, 2016 pp. 2747-2750

1.1 Autonomous Wireless Systems

- Consumed Power is the key factor
 - How much is the power that we can harvest?
 - How much power do we need for sensing?
 - How much power do we need for processing?
 - How much power do we need for transmitting?
- Budgeting Power
 - Duty cycle in the transmission mode
 - Power in the sleep mode
 - Power for analog and digital processing comparable with transmission sleep mode

2. Voltage Management

Content

- 2.1 Voltage Conversion
- 2.2 Low-Drop Voltage Regulator
- 2.3 Low-Drop Voltage Regulator (LDO)
- 2.4 Capacitive DC-DC converters
- 2.5 SIMO and SIDO DC-DC Converters
- 2.6 Low Start-up Voltage Regulators

2. Voltage Management

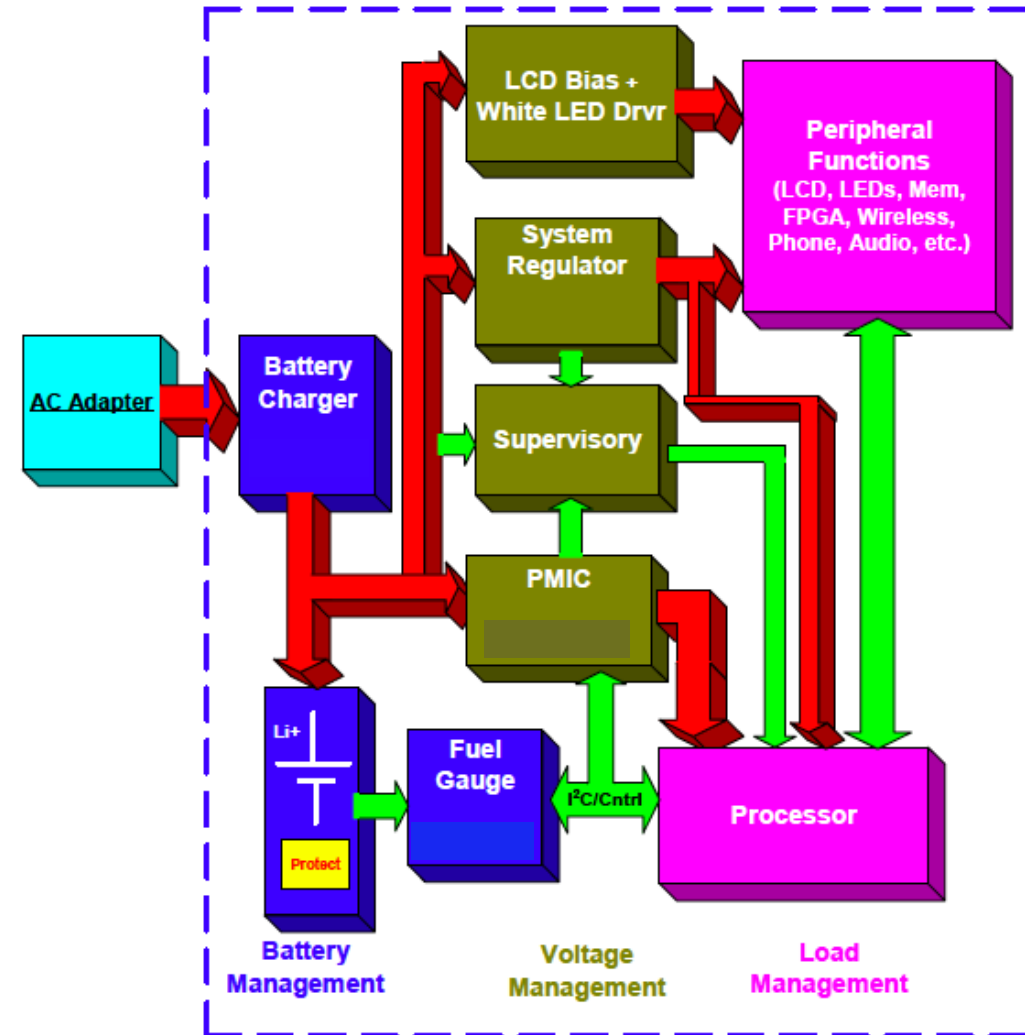
Main requirements of the voltage conversion electronics :

- Transforming the transducer electrical power into a usable voltage source
- Most of the time : voltage up-conversion (but also down-conversion or both)
- Sometimes : AC to DC conversion
- Guaranteeing the highest power extraction efficiency in any condition
- Managing highly variable sources of energy
- Providing low quiescent power consumption either when on or off
- Protecting the system from failures or electrical shocks
- Small size, low complexity, high reliability, low cost...

2.1 Voltage Conversion

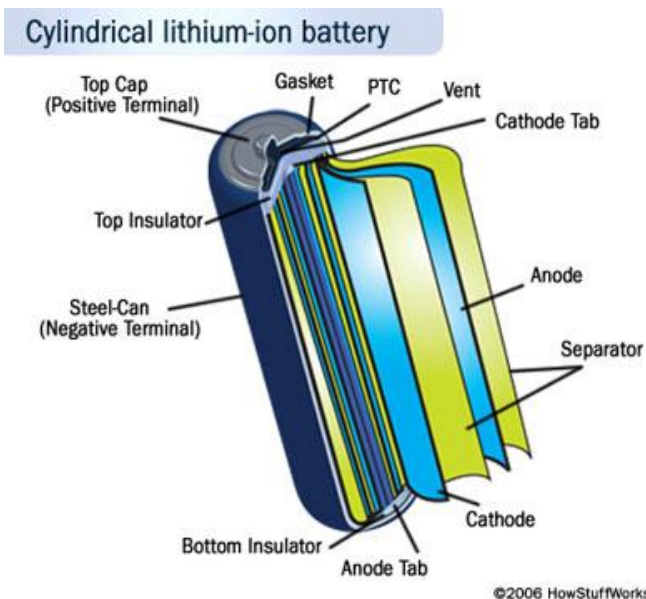
Voltage Conversion belongs to the widest area of Power Management

- **Power Management (PM)** has evolved to ever-higher levels of sophistication driven by the demands of both the applications and their users.
- Advanced power management techniques matured, and are still maturing, with the overwhelming demand for mobility and wireless connectivity that depends on reliable battery power.
- There are three interdependent areas of power management that individually and collectively affect the battery run time of the handheld device: Battery Management (BM), Voltage Management (VM) and Load Management (LM).

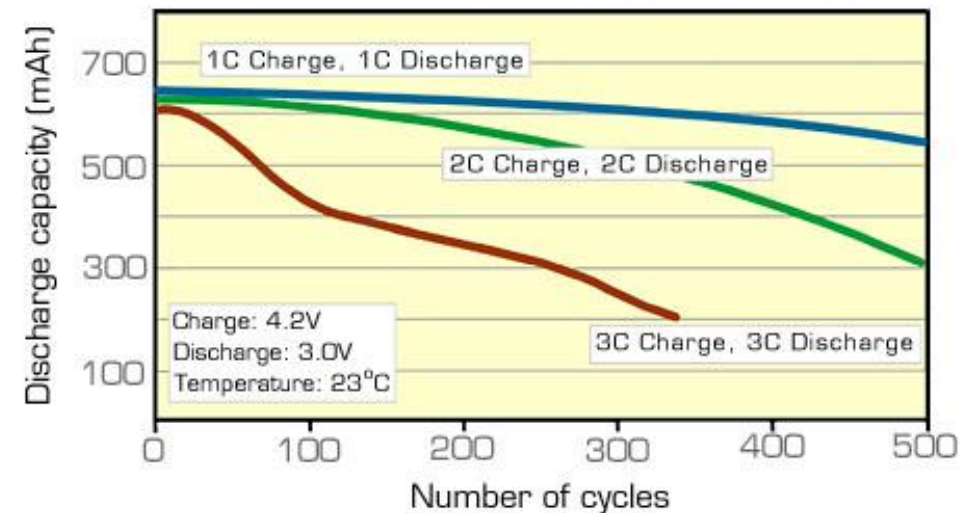


2.1 Voltage Conversion: Battery management

- **Battery Management** refers to the three primary functions of charging, protecting and monitoring the battery
- Each of these three functions perform the critical battery management goals or maximizing both the run-time per discharge cycle as well as the number of life cycles attainable for the life of the battery.
- Every Li+ battery pack is attended closely by a safety circuit that prevents any abusive condition that might result in an unsafe venting or flaming of the pack.
- The full-function BM implementation requires to perform a close monitoring function, the *fuel gauge*.

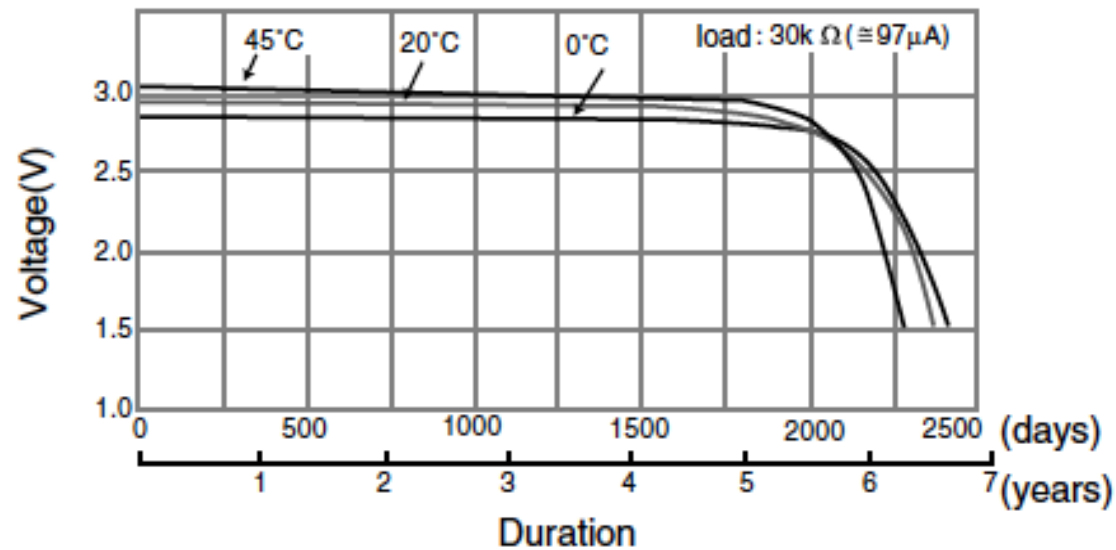


Cycle performance at various charge/discharge rates



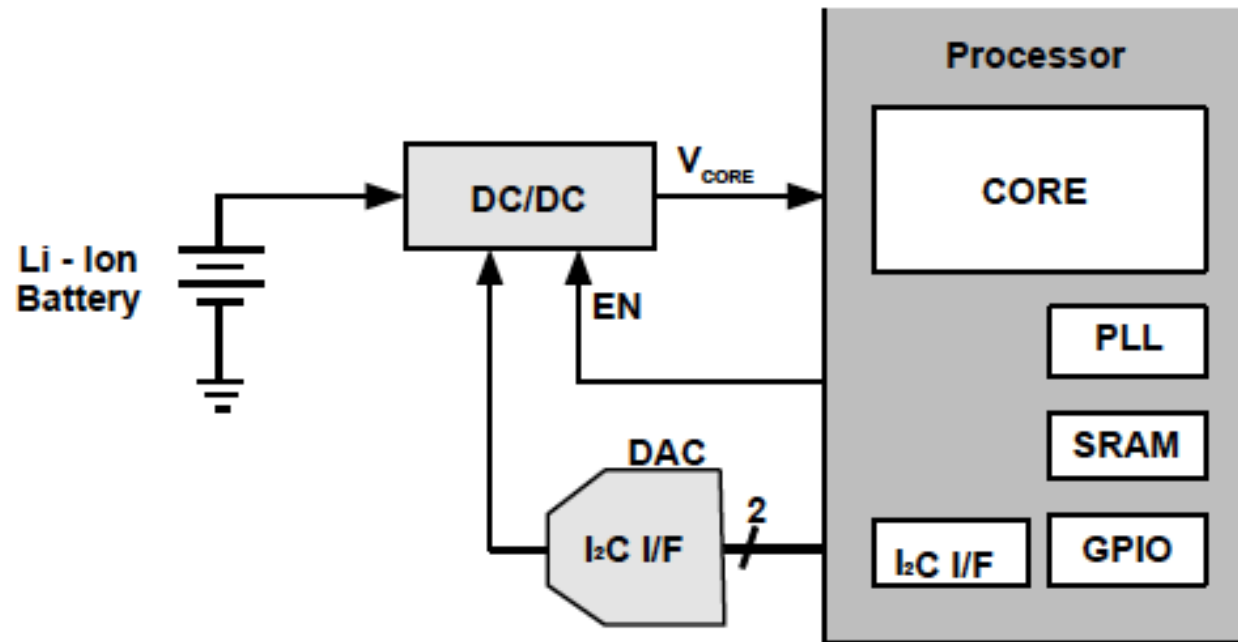
2.1 Voltage Conversion: Voltage Management

- **Voltage Management** performs the distribution/regulation function. It is responsible for efficiently conditioning the unregulated and widely varying battery voltage for compatibility with the various tight load regulation requirements
- The operative word is “efficiently”. Regulators designed specifically for handheld applications typically deliver over 90% efficiency and have very good efficiency for extended low power standby modes



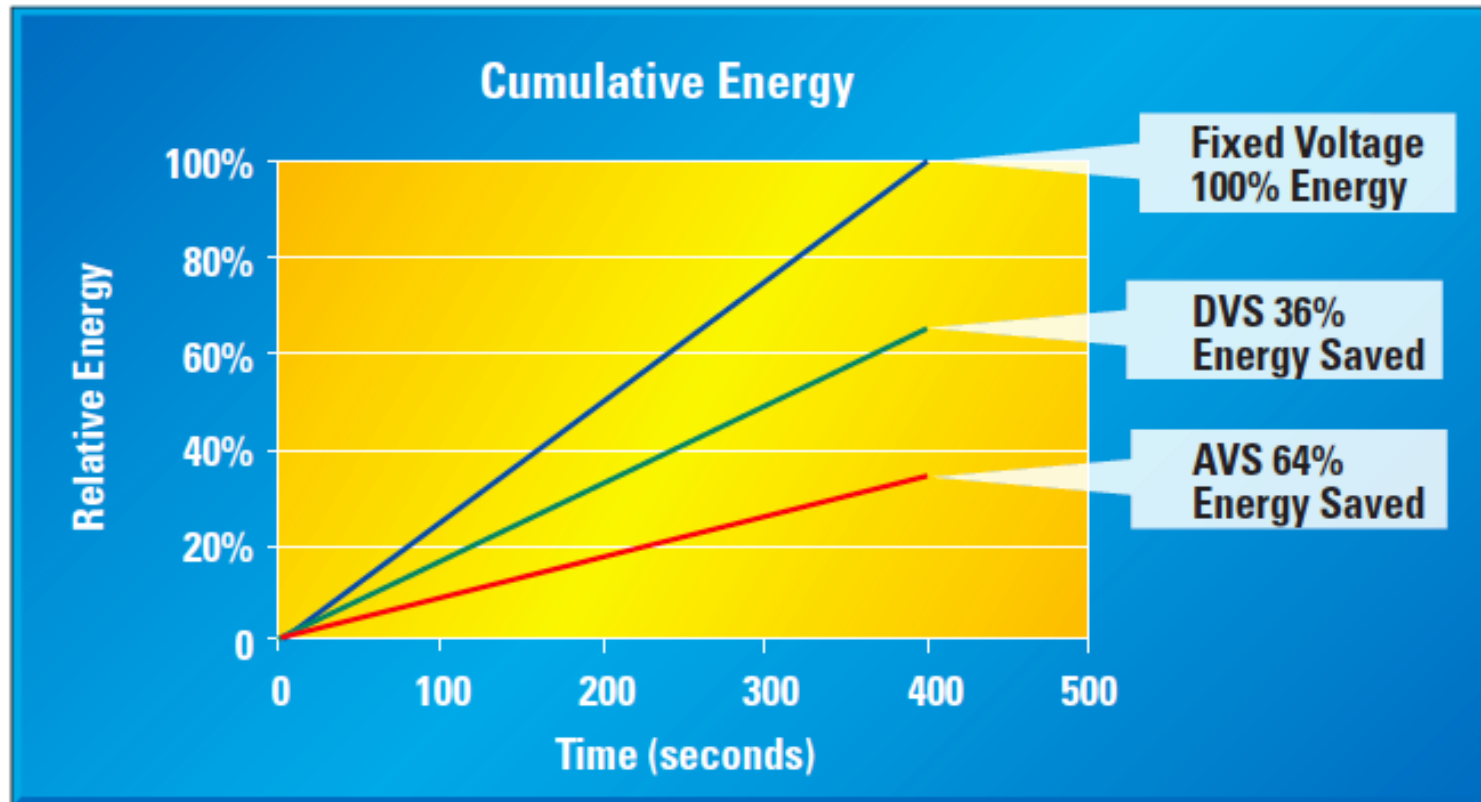
2.1 Voltage Conversion, Load Management

- **Load Management** performs a power aware delivery of power to various loads and controls the supply voltage depending on the activity and the battery voltage



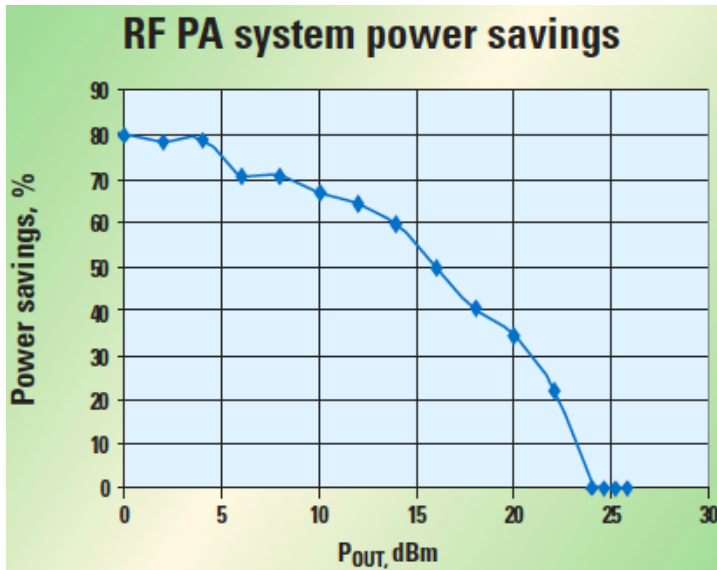
2.1 Voltage Conversion, Load Management

- Smart power management:
 - Dynamic voltage scaling (depends on the signal)
 - Adaptive voltage scaling (depends on the battery)

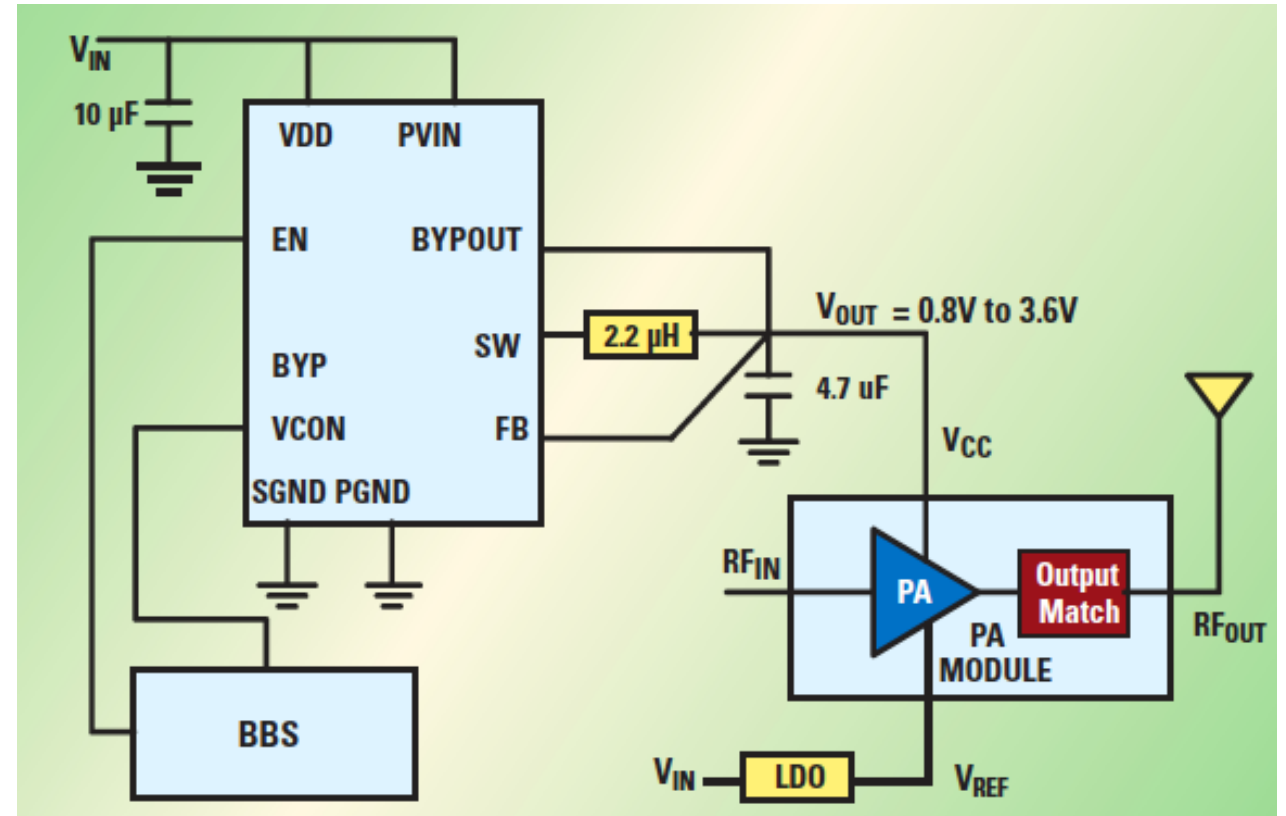


2.1 Voltage Conversion

Dynamic Voltage Scaling



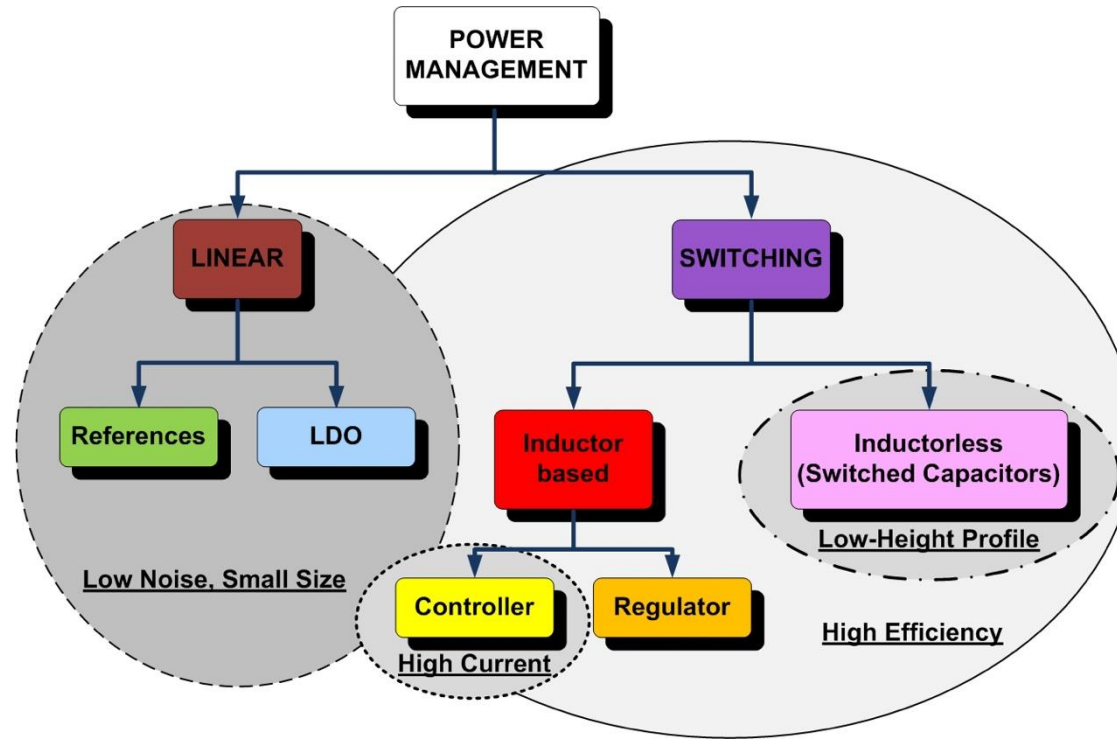
- RF power amplifier optimized for portable applications



Example of industrial implementation

2.1 Voltage Conversion: DC-DC converter

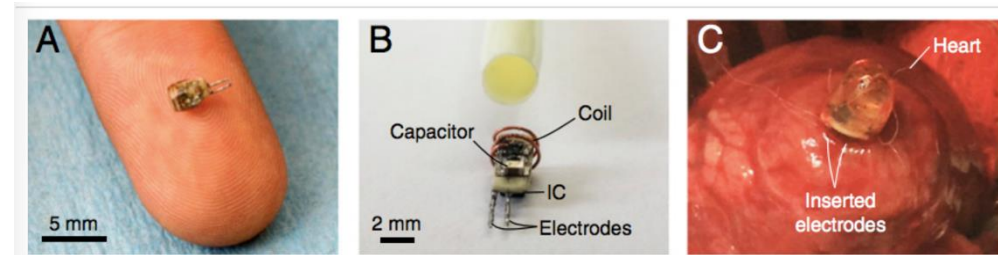
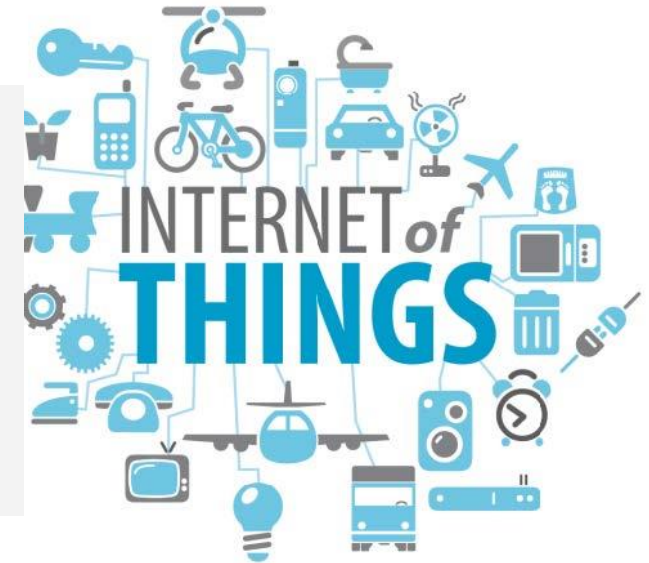
DC Voltage Regulators Topologies



	Linear	Inductive	Charge Pump
Efficiency	20-60%	90-95%	50-70%
PCB Area and cost	Very Small 2 Capacitors	Largest Big Inductor, 2 Capacitors	Medium 3-4 Capacitors
Ripple	Very Low	Low	Moderate

Portable Power Management is for

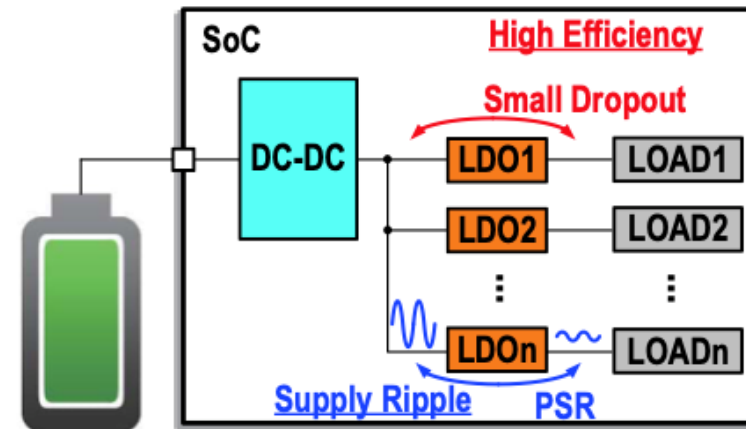
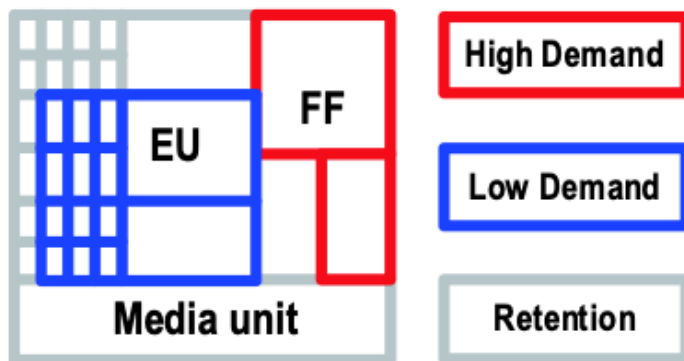
- Portable electronics battery life
- Recharging time
- Autonomous system ultra low-power
- Power supply size/weight
- Wearable electronics



2.1 Voltage Conversion: DC-DC converter

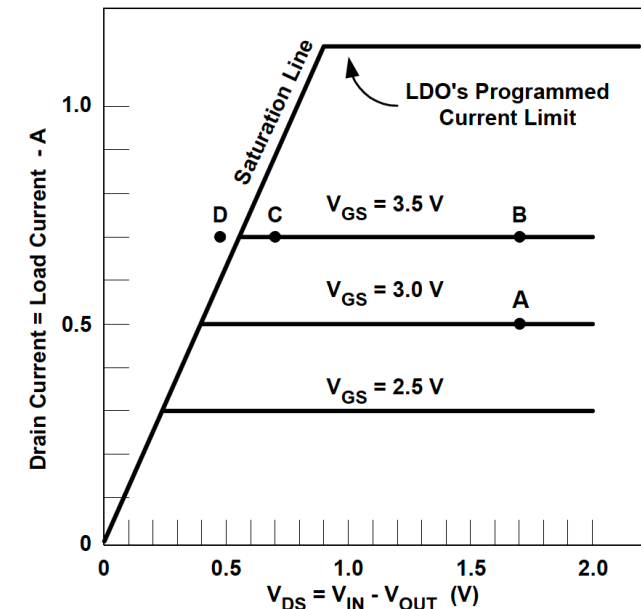
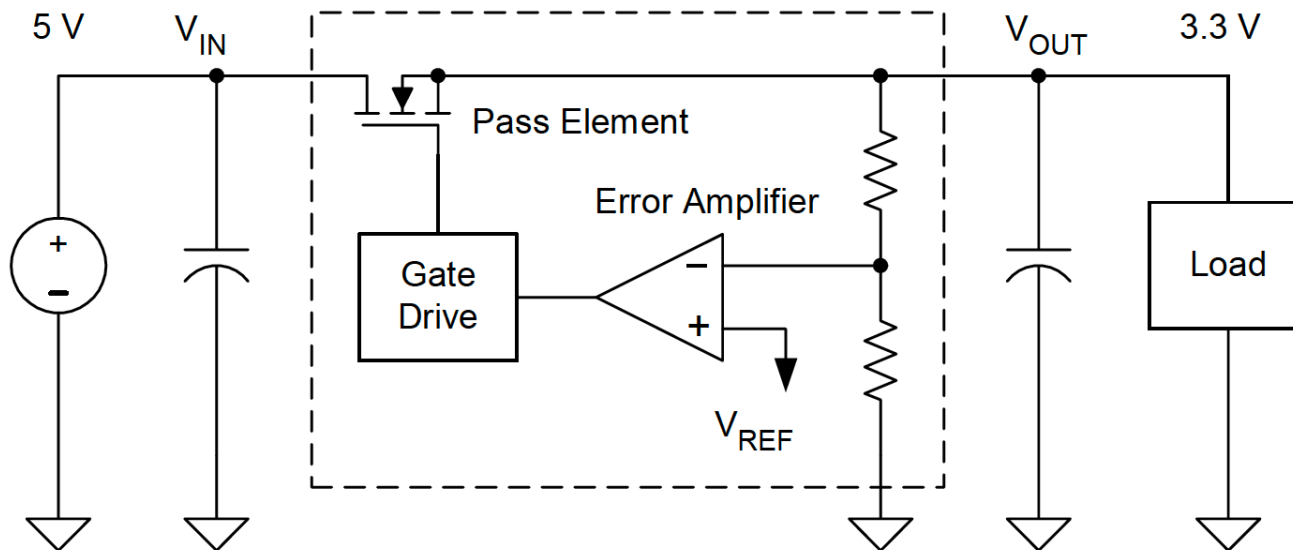
Power management is SoC

- Resources in system-on-a-chip (SoC) are highly dynamic. There are as execution units (EUs), fixed functions (FFs), and media units that can be in high demand, low demand, or retention modes.
- A good system energy efficiency uses individual supply voltage domains for different units, each with a voltage regulator: granular power management
- Granular power management in a power-efficient system on a chip (SoC) requires multiple integrated voltage regulators with a small area, process scalability, and low supply voltage.

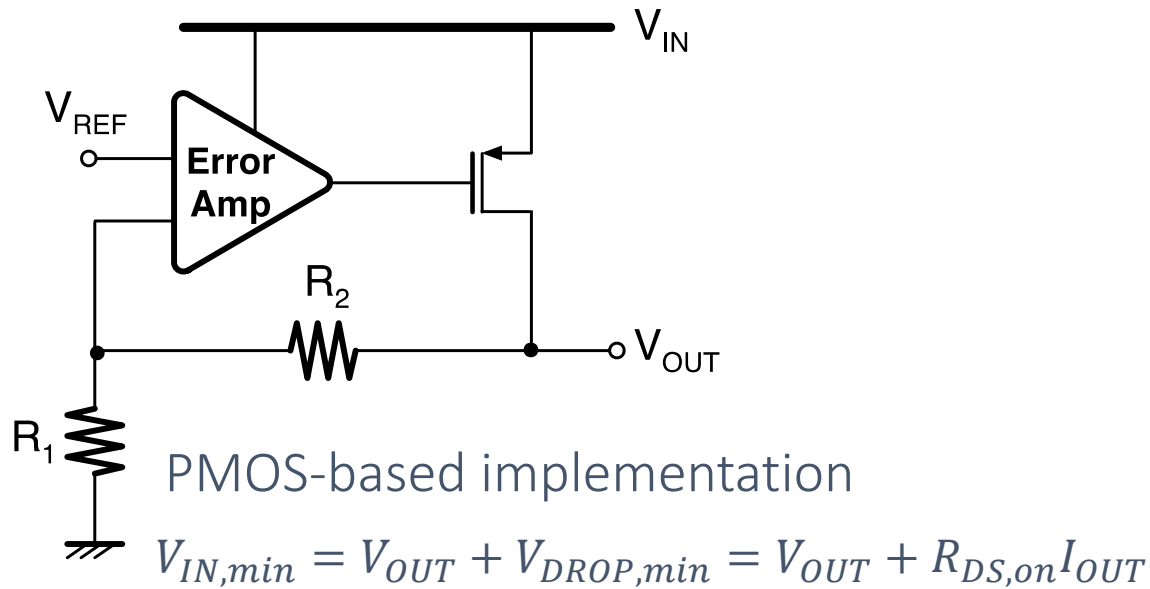


2.2 Low-Drop Voltage Regulator (LDO)

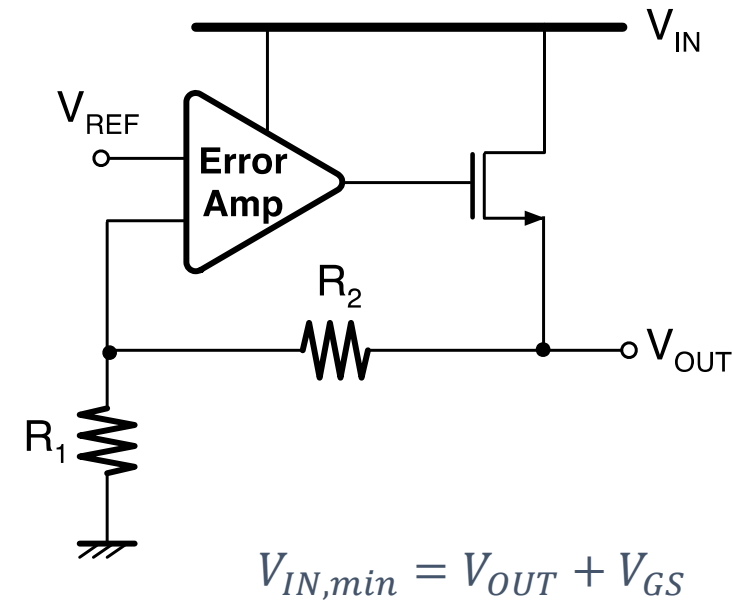
- The scheme uses a pass element (NMOS or PMOS). The pass element behaves like a simple resistor to drop the input voltage down to the desired output voltage, sensed by the error amplifier and compared to the reference voltage. As the operating current or input voltage changes, the error amplifier modulates the pass element to maintain an almost constant output voltage.



2.2 Low-Drop Voltage Regulator (LDO)



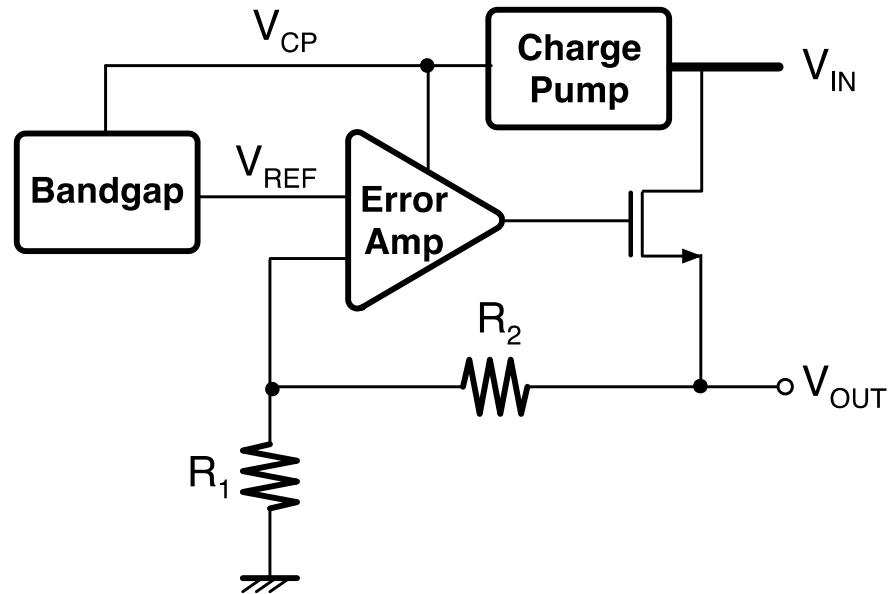
- Very low dropout voltage ✓
- Good PSRR ✓
- Extra gain stage difficult compensation ✗
- Bad performance at low supply ✗



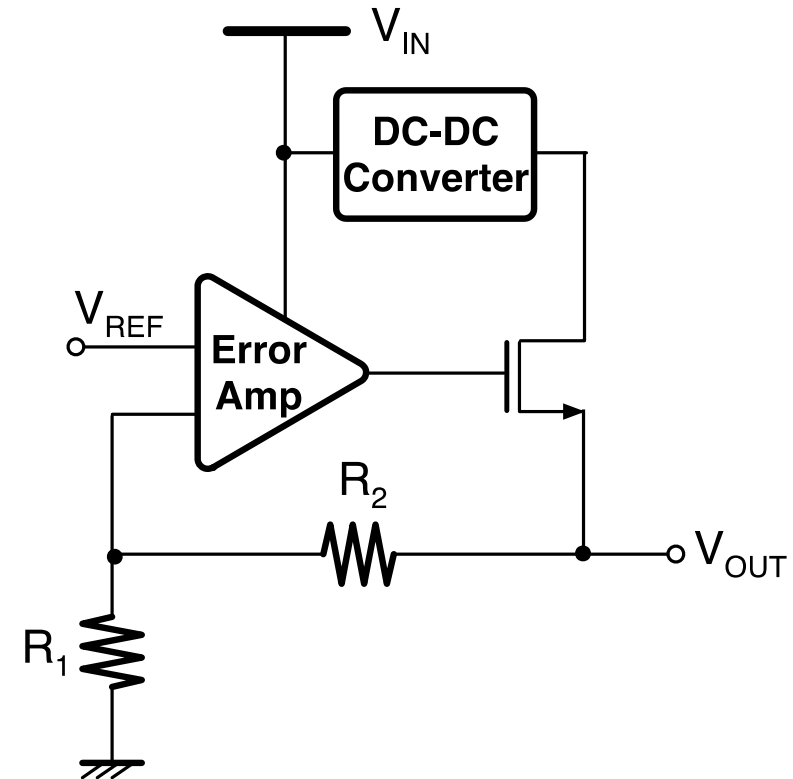
- Easy to get the loop stability ✓
- Speed: immediate response of any load variation ✓
- NMOS ensures smaller area, and smaller parasitic ✓
- The dropout is large or requires boosting ✗

2.2 Low-Drop Voltage Regulator (LDO)

Boosting of supply of the error amplifier



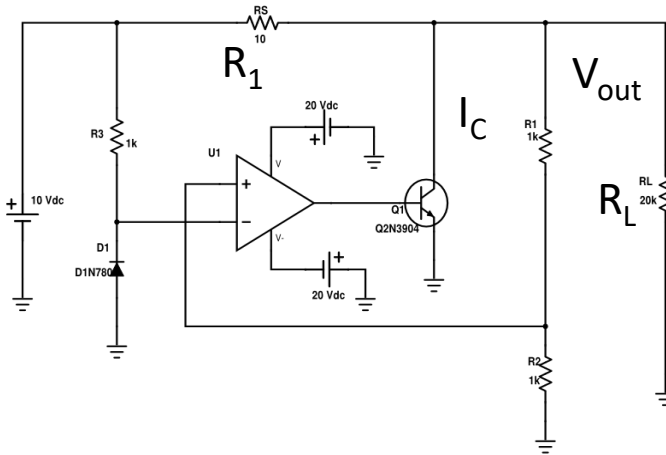
Cascade of DC-DC and LDO



2.2 Low-Drop Voltage Regulator (LDO)

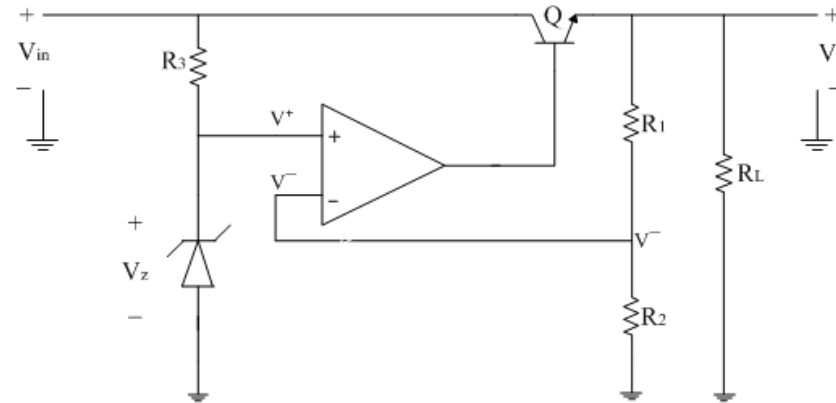
Possible spur on the supply voltage are badly rejected, especially at high frequency.

The LDO determines a drop of the input voltage to obtain a clean lower supply voltage.



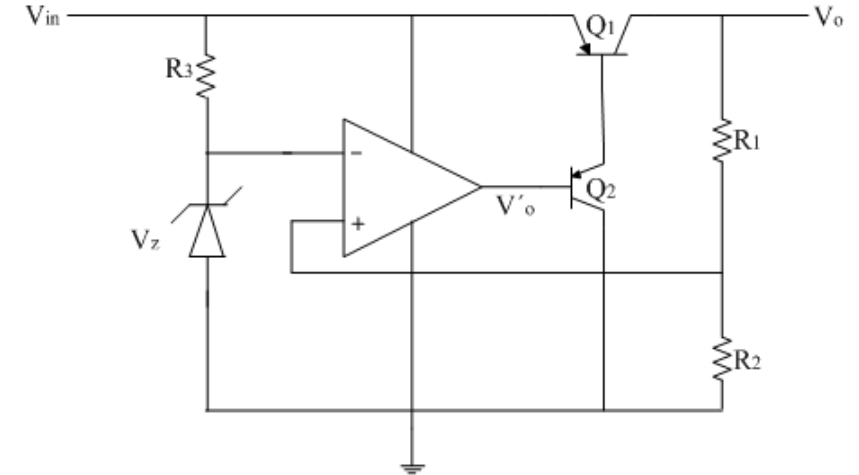
Shunt Voltage regulator

Efficiency drops for large R_L



Emitter follower regulator

Efficiency drops when $V_{in} - V_{out}$ is a large fraction of V_{in}



Amplifier type regulator

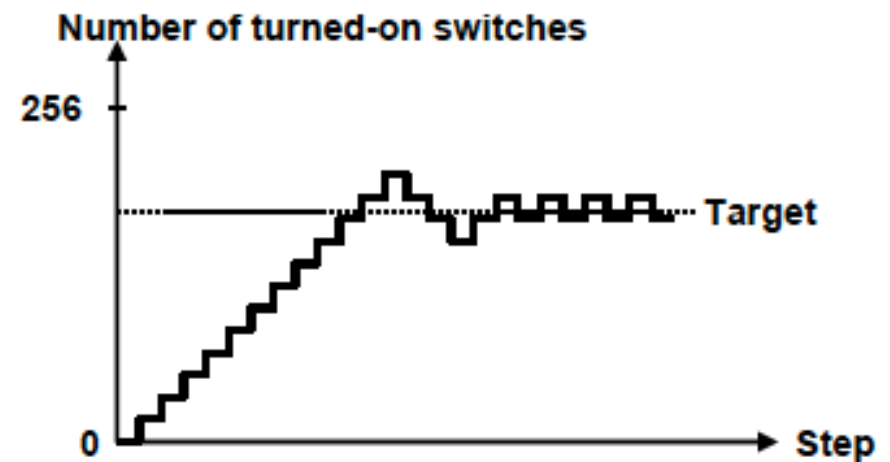
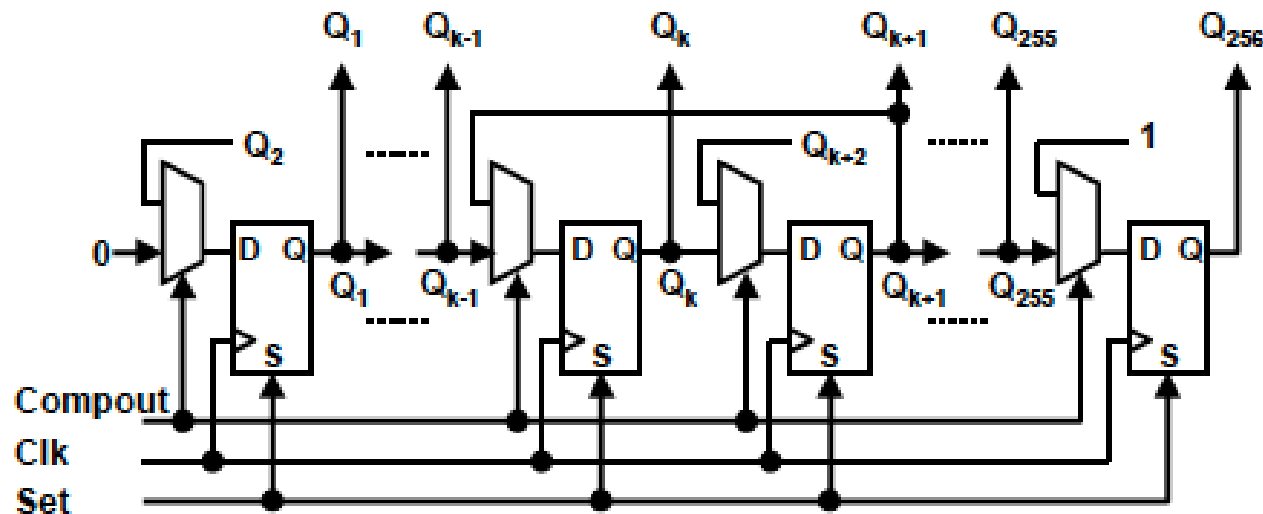
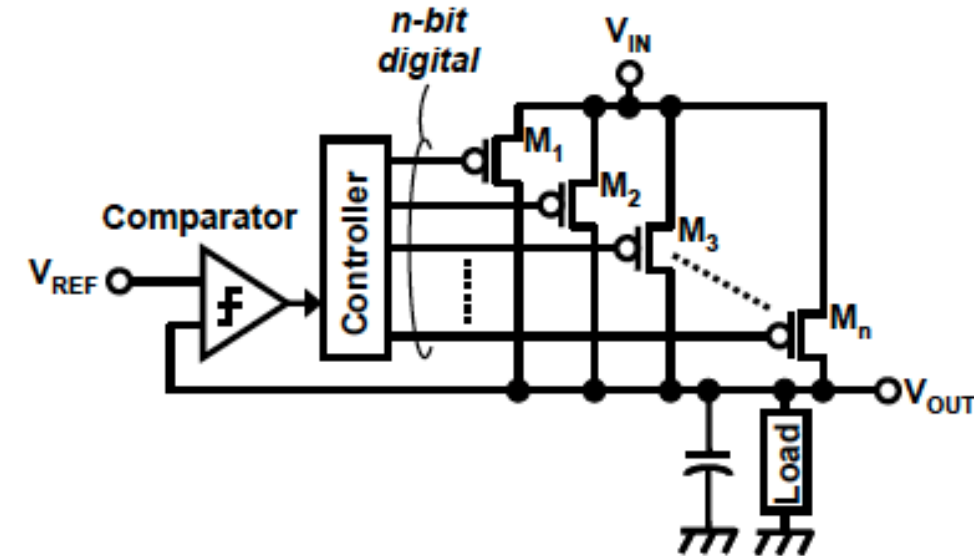
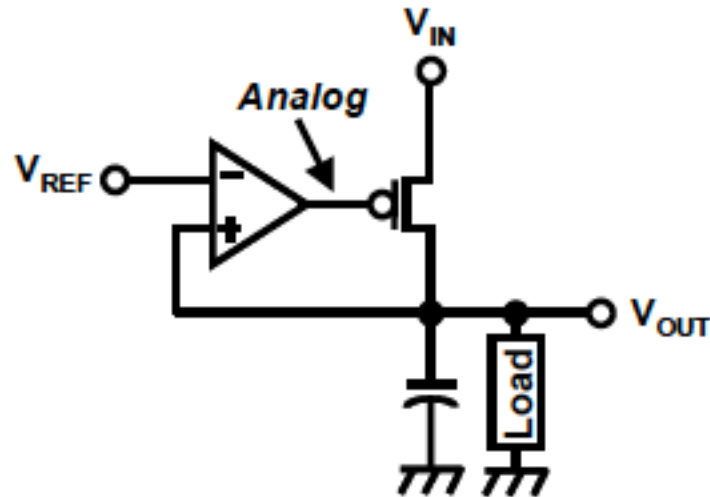
Equivalent schemes with MOS transistors

2.2 Low-Drop Voltage Regulator (LSC)

For low voltages the required overhead cannot be provided

DIGITAL LDO

Y. Okuma, et al., "0.5-V Input Digital LDO with 98.7% Current Efficiency and 2.7- μ A Quiescent Current in 65nm CMOS," IEEE CICC, 2010.



2.1 Voltage Conversion: DC-DC converter

Digital LDO

Power speed trade-off

USE A FIGURE OF MERIT

$$\text{FOM} = T_R \frac{I_Q}{I_{\text{MAX}}} = \frac{C_{\text{OUT}} \cdot \Delta V_{\text{OUT}}}{I_{\text{MAX}}} \cdot \frac{I_Q}{I_{\text{MAX}}},$$

T_R is the transient response time

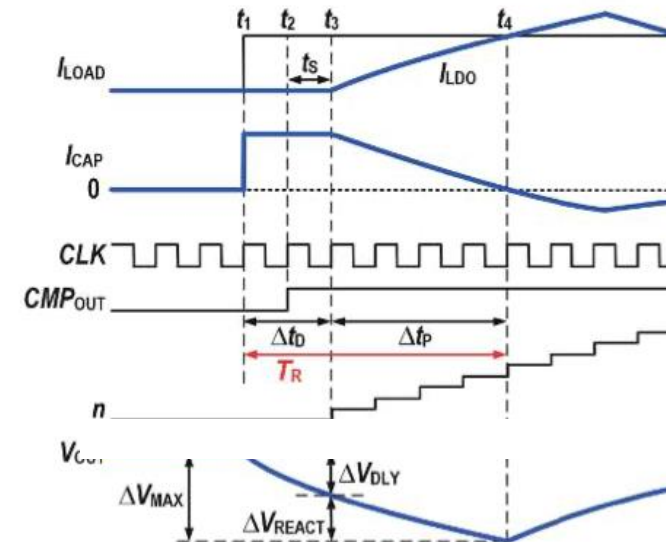
I_Q is the quiescent current

I_{MAX} is the maximum load current

C_{OUT} is output capacitor

ΔV_{OUT} is the output voltage spike with the I_{MAX} load step.

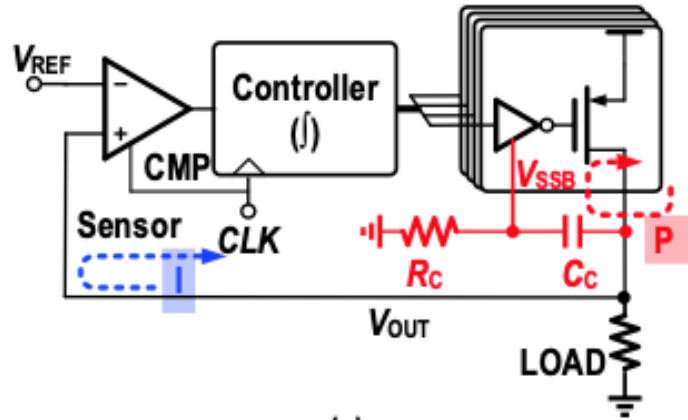
For an analog LDO, the bandwidth of the LDO loop and slew rate determine the T_R . It is inversely proportional to the I_Q . Multiple-loop schemes can reduce T_R without significantly increasing I_Q .



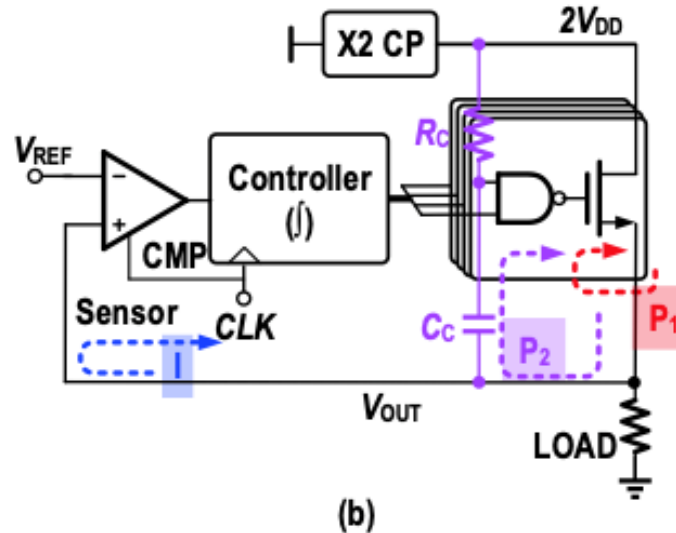
The synchronous digital LDO has a long T_R causing a slower transient response.

Techniques that also use digital processing allow improving T_R .

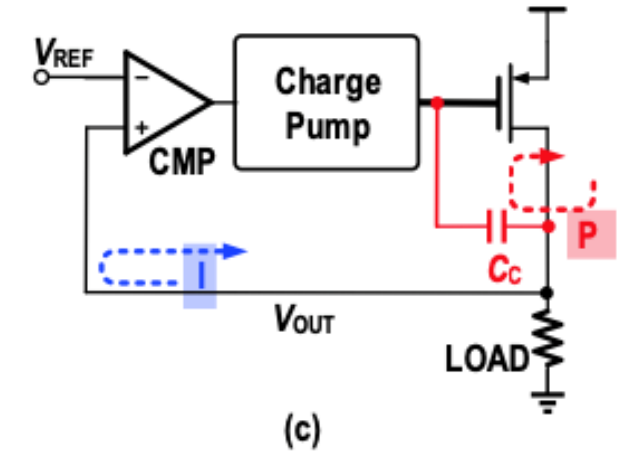
2.2 Low-Drop Voltage Regulator (LSC)



Huang M, Lu Y, Seng-Pan U, et al. An output-capacitor-free analog-assisted digital low-dropout regulator with tri-loop control. 2017 IEEE International Solid-State Circuits Conference (ISSCC), 2017, 342



Ma X F, Lu Y, Martins R P, et al. A 0.4 V 430 nA quiescent current NMOS digital LDO with NAND-based analog-assisted loop in 28 nm CMOS. 2018 IEEE International Solid-State Circuits Conference (ISSCC), 2018, 306



Wang X Y, Mercier P P. A dynamically high-impedance charge-pump-based LDO with digital-LDO-like properties achieving a sub-4-fs FoM. *IEEE J Solid-State Circuits*, 2020, 55, 719

Hybrid LDO

Nasir S B, Sen S, Raychowdhury A. Switched-mode-control based hybrid LDO for fine-grain power management of digital load circuits. *IEEE J Solid-State Circuits*, 2018, 53, 569

JOURNAL OF SEMICONDUCTORS 2020

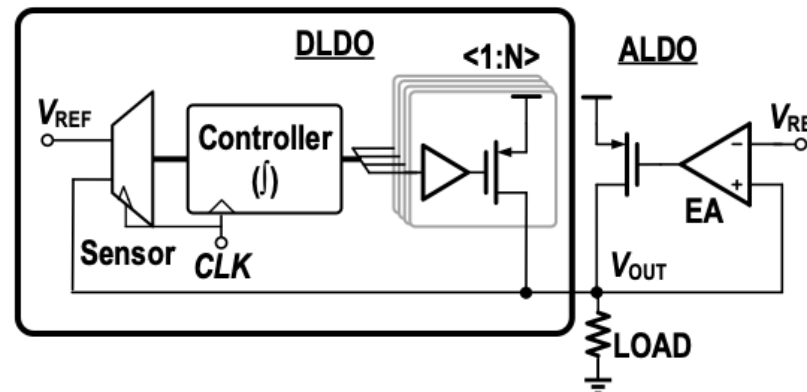
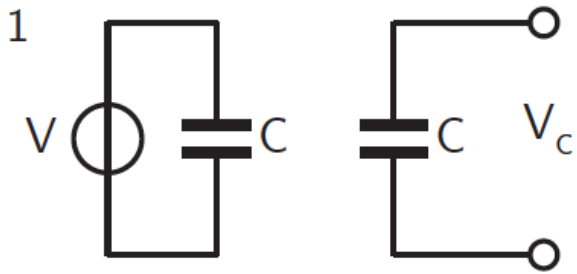


Table 2. FoM of speed versus process nodes.

Year	Process (nm)	Architecture	FoM (ps)
2020 ^[39]	130	ADC + PID	63.9
2016 ^[22]	65	ADC + Event driven	20
2016 ^[21]	28	ADC + Coarse/fine	9.57
2020 ^[40]	20	ADC + Computational	6.7
2020 ^[36]	10	TDC + PID	5.2
2017 ^[15]	65	Analog-assisted	0.23
2018 ^[18]	28	Analog-assisted	0.026

2.3 Capacitive DC-DC Converter

Basic Concepts: switching capacitors



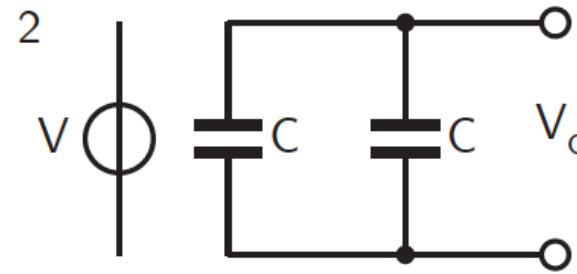
■ $V_{C,1} = 0$

■ $E_1 = \frac{1}{2}CV^2$

😊 $V_{C,1} \neq V_{C,2} \rightarrow$ Voltage conversion

☹️ $E_2 \leq E_1 \rightarrow$ Charge sharing losses ($CV^2/4$)

■ Whenever charge sharing occurs some energy is lost even under ideal conditions



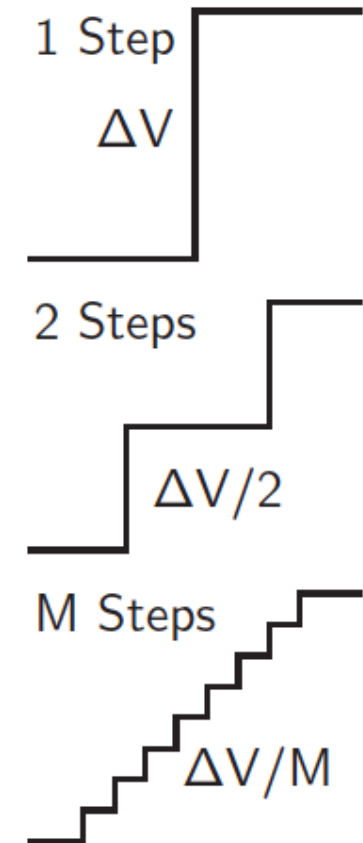
■ $V_{C,2} = V/2$

■ $E_2 = \frac{1}{4}CV^2$

2.3 Capacitive DC-DC Converter

Basic Principle — Interesting Consideration

- Charge sharing losses are proportional to ΔV_C^2
 - $\Delta E = C\Delta V_C^2$
- If ΔV_C is achieved with two consecutive steps with amplitude $\Delta V_C/2$ each
 - $\Delta E_1 = C\Delta V_C^2/4$ and $\Delta E_2 = C\Delta V_C^2/4$
 - $\Delta E = \Delta E_1 + \Delta E_2 = C\Delta V_C^2/2$
- If ΔV_C is achieved with M consecutive steps with amplitude $\Delta V_C/M$ each
 - $\Delta E_i = C\Delta V_C^2/M^2$ for $i = 1, \dots, M$
 - $\Delta E = \sum_{i=1}^M \Delta E_i = C\Delta V_C^2/M$
- For $M \rightarrow \infty \rightarrow \Delta E \rightarrow 0$ (adiabatic charging)



2.3 Capacitive DC-DC Converter

SWITCHED CAPACITOR BASED

- Most important SCC topologies
 - Ladder topology
 - Fibonacci topology
 - Cockcroft-Walton multiplier
 - Dickson charge pump
 - Series-parallel topology
 - Voltage doubler topology
- All of these SCC topologies are bidirectional
 - Step-down SCC → $V_{in} = V_H$, $V_{out} = V_L$, conversion ratio → $n : 1$
 - Step-up SCC → $V_{in} = V_L$, $V_{out} = V_H$, conversion ratio → $1 : n$
- The conversion ratio n or $1/n$ depends on the number of capacitors
 - The more capacitors are used the larger is n in any SCC topology
 - The number of capacitors required for achieving a certain n depends on the SCC topology

2.3 Capacitive DC-DC Converter

Topologies — Example: 1 : 2 SCC

■ Phase 1

- $Q_C = V_{in} C$

- $Q_1 = \sum_i Q_{C,i} = V_{in} C$

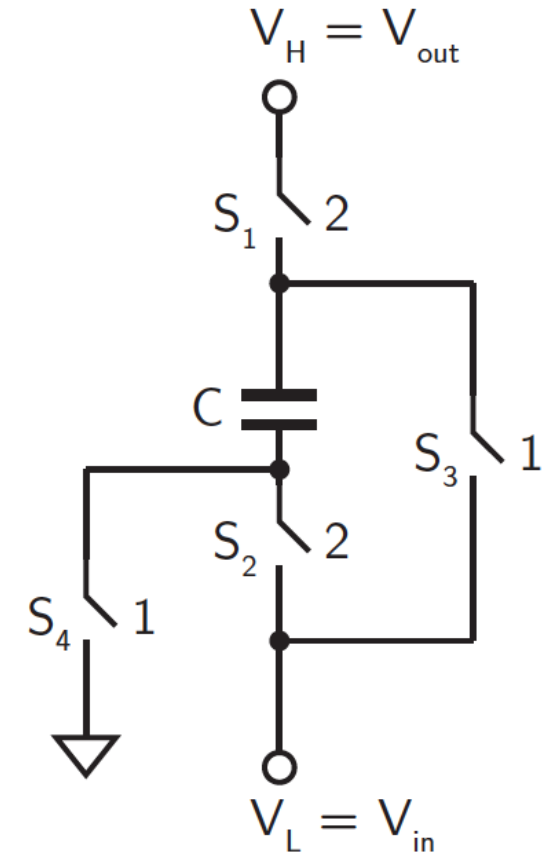
■ Phase 2

- $Q_C = (V_{out} - V_{in}) C$

- $Q_2 = \sum_i Q_{C,i} = (V_{out} - V_{in}) C$

- $Q_1 = Q_2$ (Steady state → No charge transfer)

- $V_{out} = 2V_{in}$



2.3 Capacitive DC-DC Converter

Topologies — Example: 3 : 1 Dickson SCC

- $C_1 = C_2 = C$

- Phase 1

- $Q_{C_1} = \frac{V_{out}}{2} C$

- $Q_{C_2} = \frac{V_{out}}{2} C$

- $Q_1 = \sum_i Q_{C,i} = V_{out} C$

- Phase 2

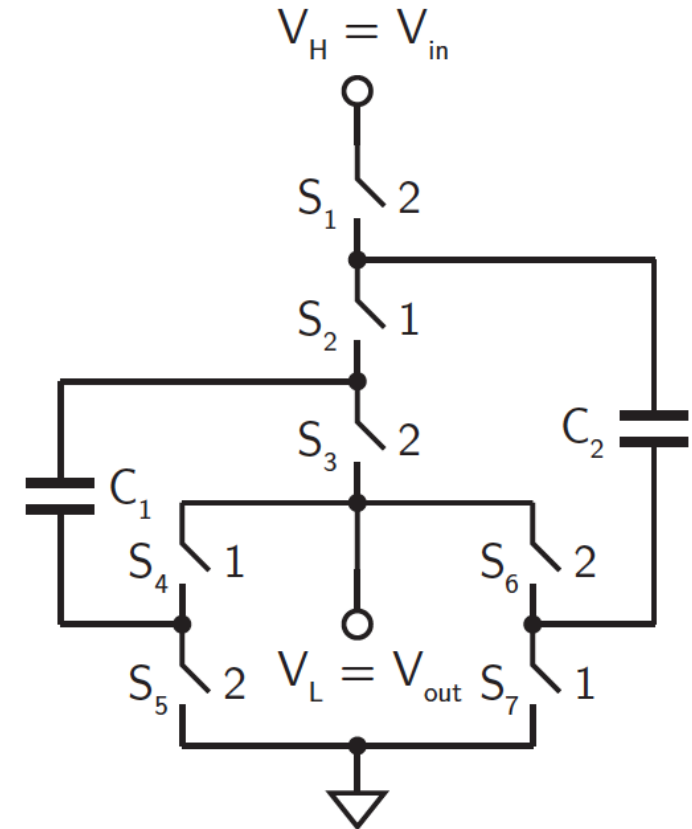
- $Q_{C_1} = -V_{out} C$

- $Q_{C_2} = (V_{in} - V_{out}) C$

- $Q_2 = \sum_i Q_{C,i} = (V_{in} - 2V_{out}) C$

- $Q_1 = Q_2$ (Steady state → No charge transfer)

- $V_{out} = \frac{V_{in}}{3}$

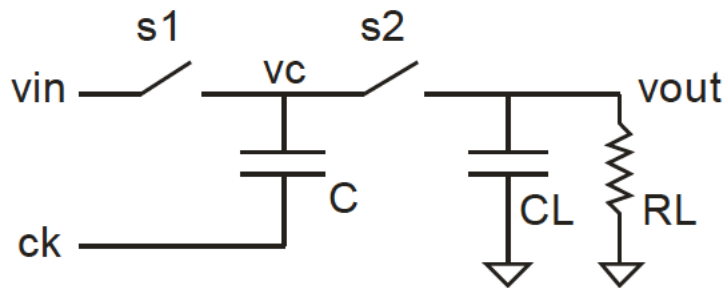


2.3 Capacitive DC-DC Converter

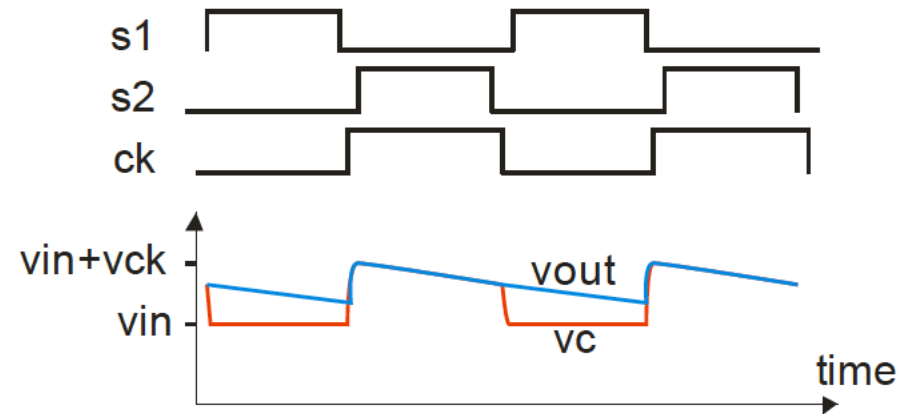
Useful charge pump basic cell

A second switch is required to discharge C in the load

Circuit



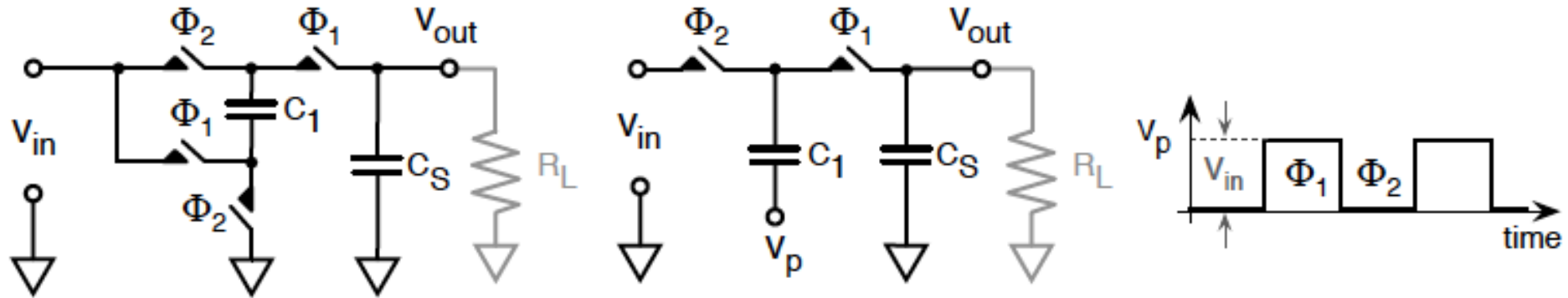
Timing and output voltage



Output ripple decreases when f (operating frequency) or C_L increase.

2.3 Capacitive DC-DC Converter

Charge Pump



$$Q_{1,j} = C_1 V_{in} \quad ; \quad Q_{S,j} = C_S V_{out}(j).$$

$$V_{out}(j) = 2 \frac{C_1}{C_1 + C_S} V_{in} + \frac{C_S}{C_1 + C_S} V_{out}(j-1).$$

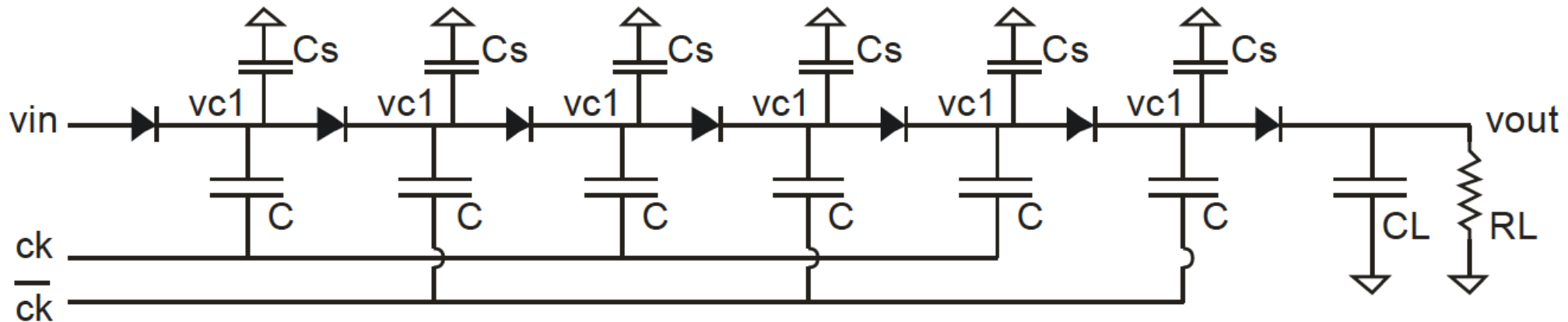
$$V_{out} = 2 \frac{C_1}{C_1 + C_S} V_{in} + \frac{C_S}{C_1 + C_S} V_{out},$$

$$V_{out} = 2 V_{in}.$$

2.3 Capacitive DC-DC Converter

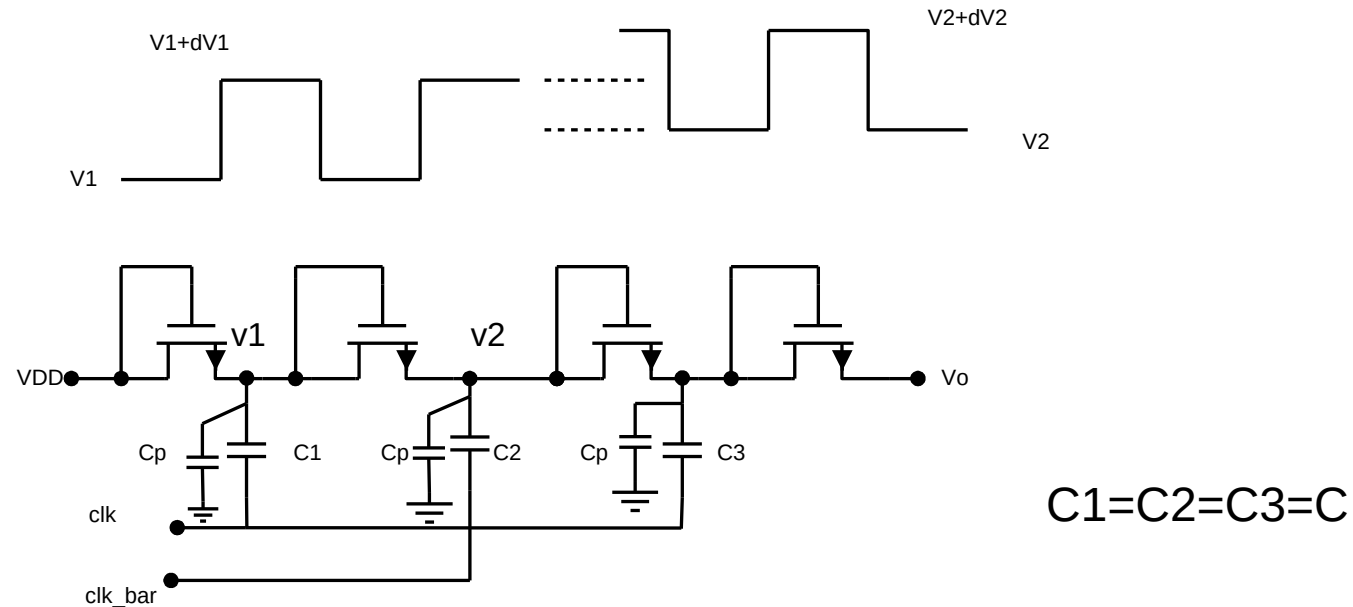
The Dickson charge pump (II)

A high number of stages can be cascaded to obtain high output voltage.
The output voltage is limited by capacitor breakdown voltage.



2.3 Capacitive DC-DC Converter

REPLACING DIODES WITH MOS TRANSISTORS



$$\Delta V = V_{\phi} \frac{C}{C + C_p} - \frac{I_o}{f(C + C_p)}$$

$$\Delta V > V_{th} \quad (\text{Body effect can be significant at later stages})$$

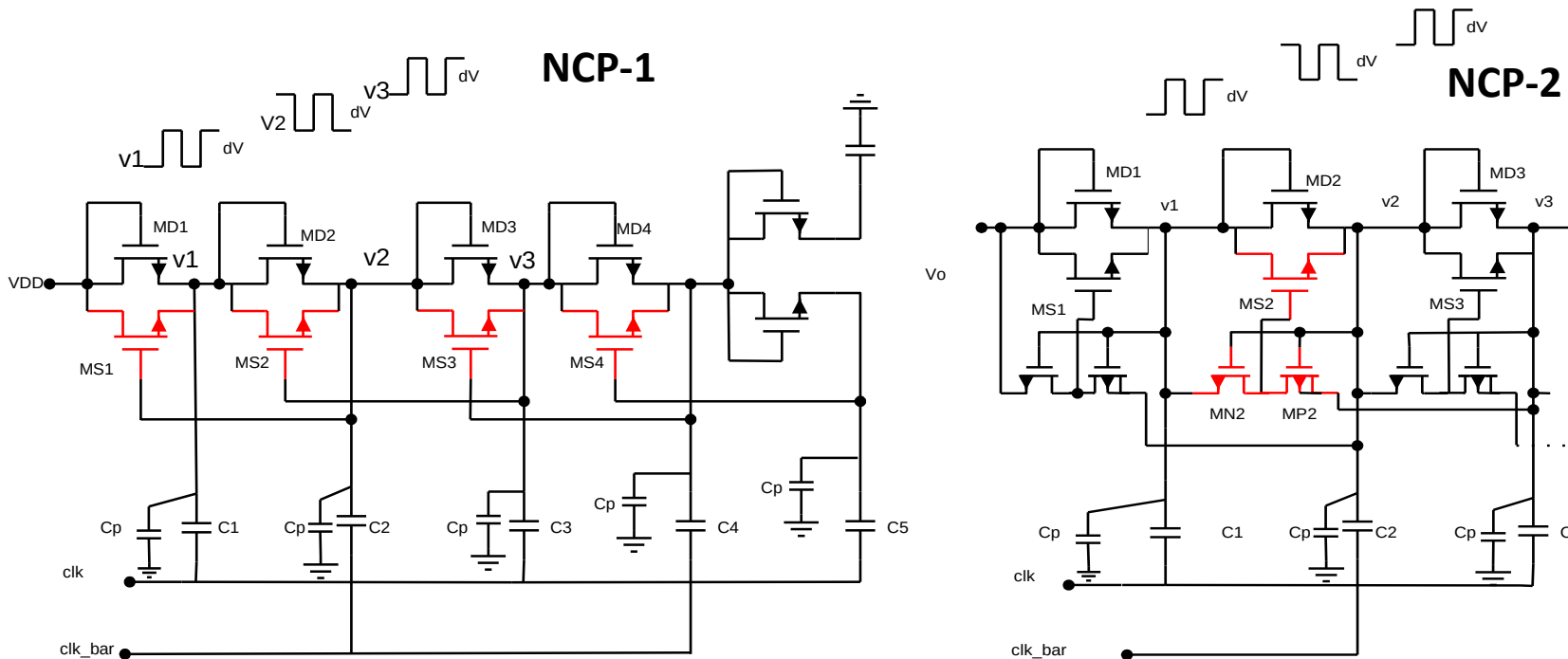
$$V_{out} = V_{DD} + N * (\Delta V - V_t) - V_t$$

2.3 Capacitive DC-DC Converter

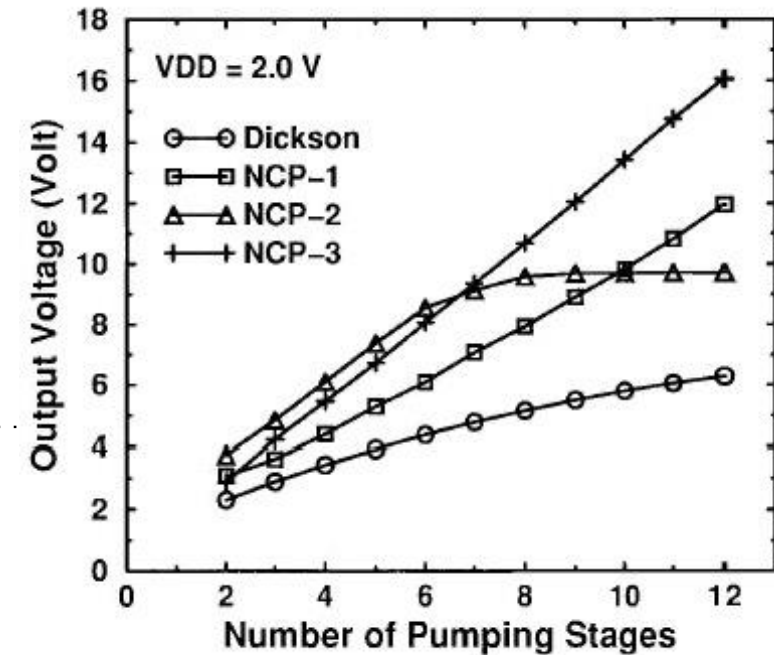
REPLACING DIODES WITH MOS TRANSISTORS

- Threshold voltage drop [MOS charge pumps for low-voltage operation]

$$V_{th} = V_{tho} + \gamma \left(\sqrt{V_{BS} + 2\phi_F} - \sqrt{2\phi_F} \right)$$



NCP-3= NCP'' + boosted CLK out



2.3 Capacitive DC-DC Converter

Replacing diodes with switches

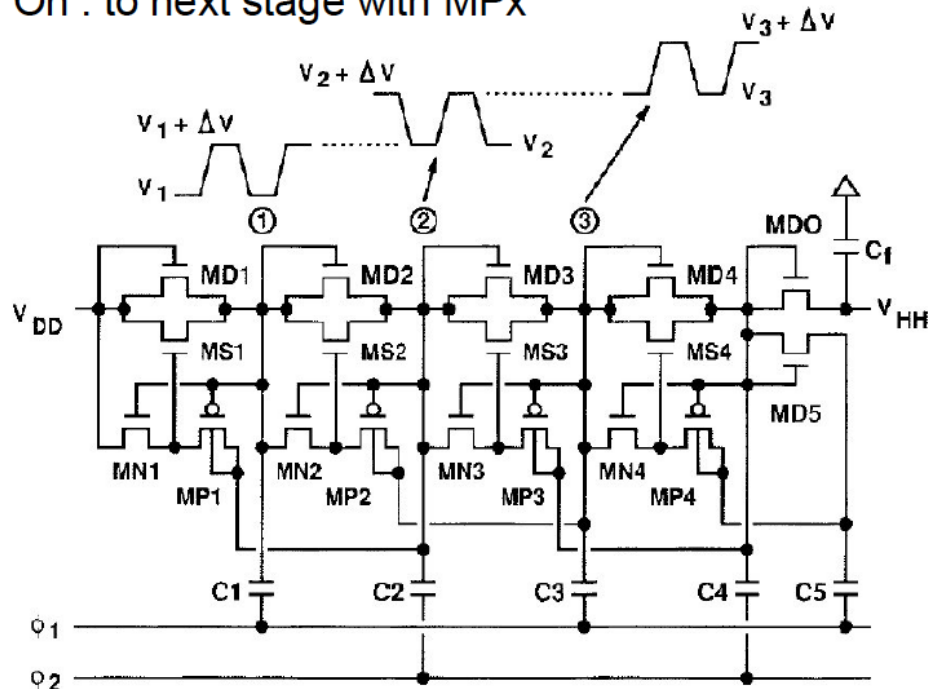
Jieh-Tsorng Wu, Kuen-Long Chang, "MOS Charge Pumps for Low-Voltage Operations", IEEE JSSC, Vol. 33, No. 4, April 1998, pp. 592-597.

MDx : used for startup only MSx : voltage transfer switch

With gate connected to adequate Voltage:

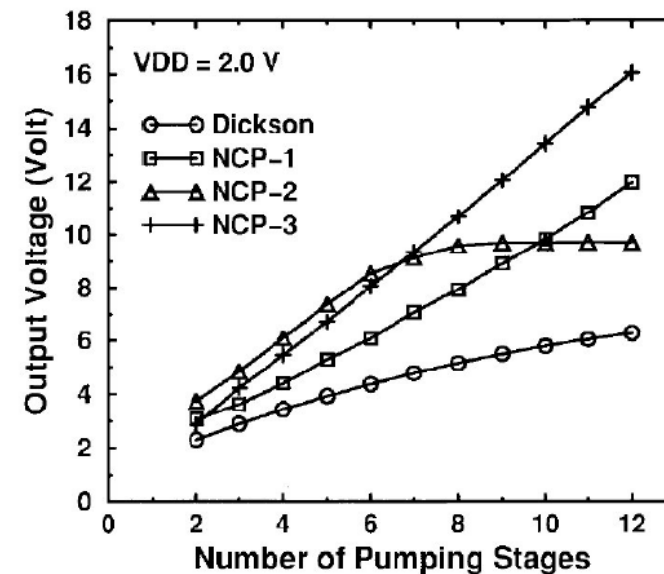
Off : to previous stage with MNx

On : to next stage with MPx



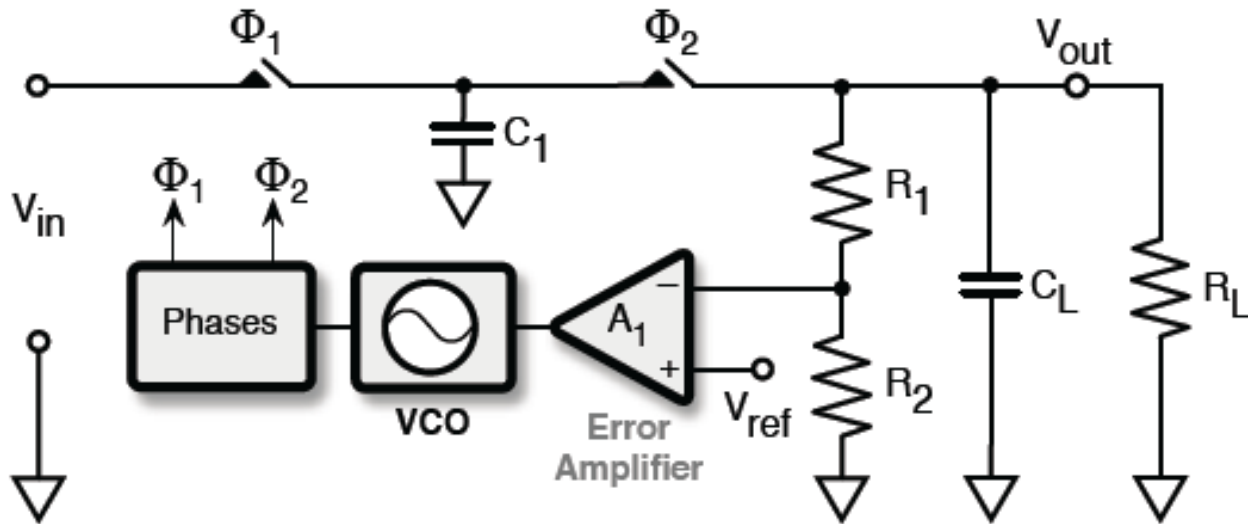
Performance of NCP-1

NCP-3 : same as NCP-1 but with improved last stage

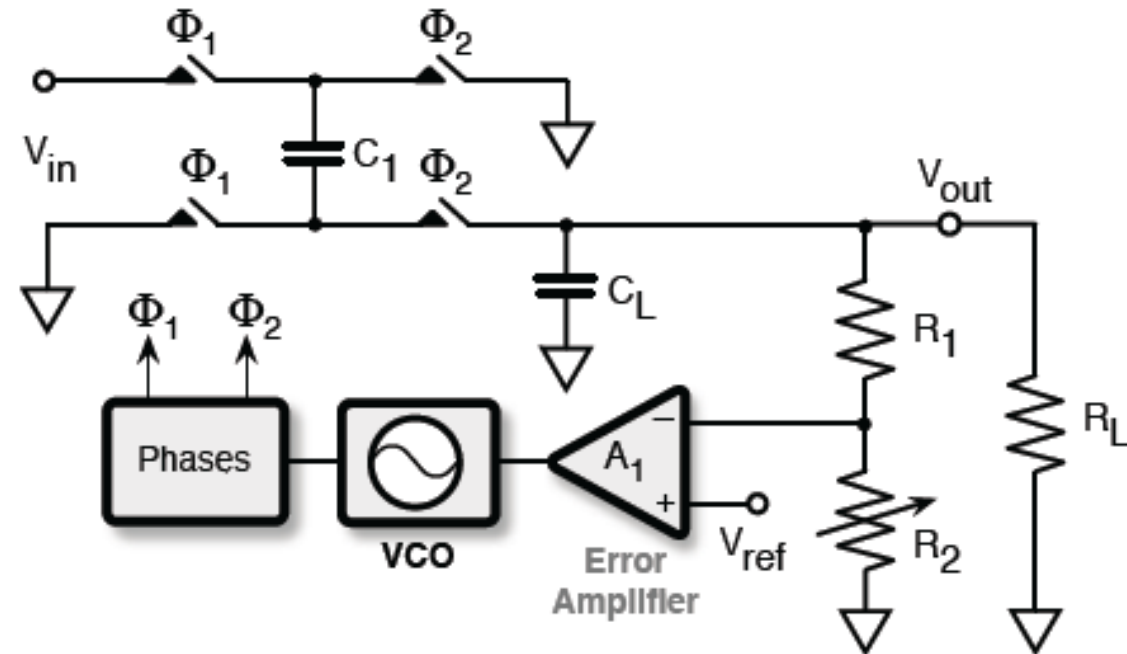


2.3 Capacitive DC-DC Converter

Switched Based regulator



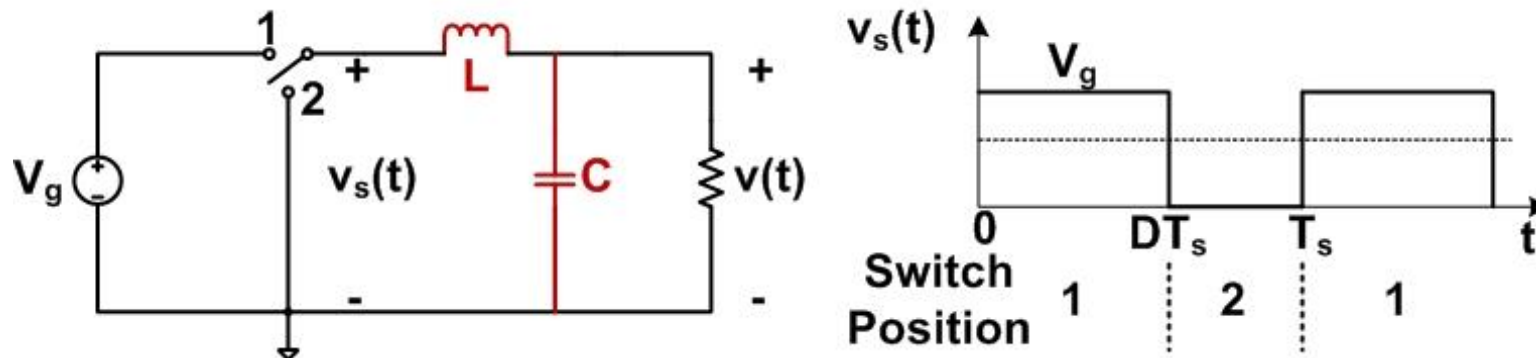
Positive output voltage



Negative output voltage

2.4 Inductive DC-DC Converter

From Duty Cycle to Buck Converter



- ❑ $D \rightarrow$ switch duty ratio, $0 \leq D \leq 1$
- ❑ From the Fourier analysis the DC component of $v_s(t)$ is:

$$\langle v_s(t) \rangle = \frac{1}{T_s} \int_0^{T_s} v_s(t) dt = \frac{1}{T_s} \cdot (DT_s V_g) = DV_g$$

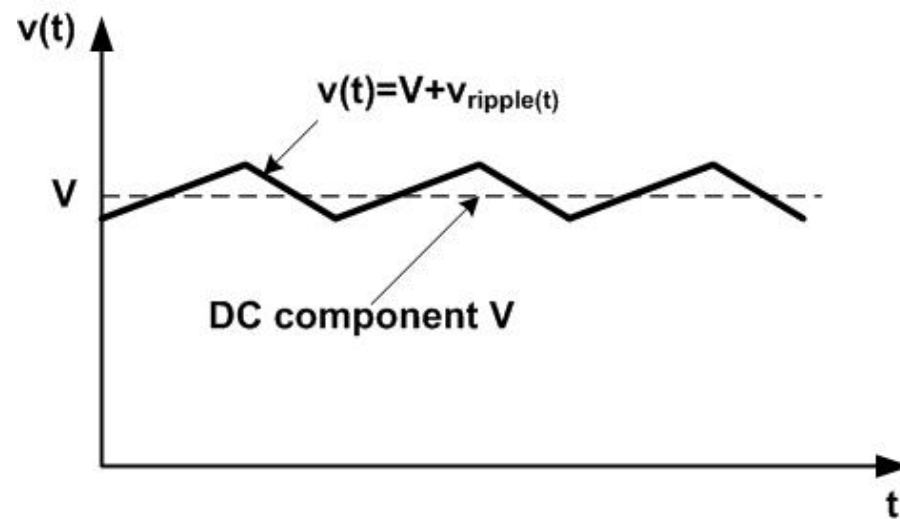
- ❑ The switch reduces the DC component of the input voltage V_g by a factor D
- ❑ LC low-pass filter to obtain DC output voltage
- ❑ Ideal lossless-elements to approach 100% power efficiency

2.4 Inductive DC-DC Converter

Small-Ripple Approximation

- ❑ Real LC low-pass filter partially rejects switching frequency and its harmonics
- ❑ Output voltage consist of the desired DC component, plus a small undesired AC component:

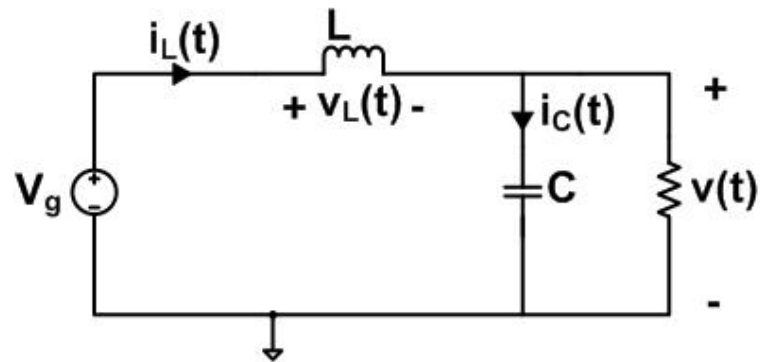
$$v(t) = V + v_{\text{ripple}}(t)$$



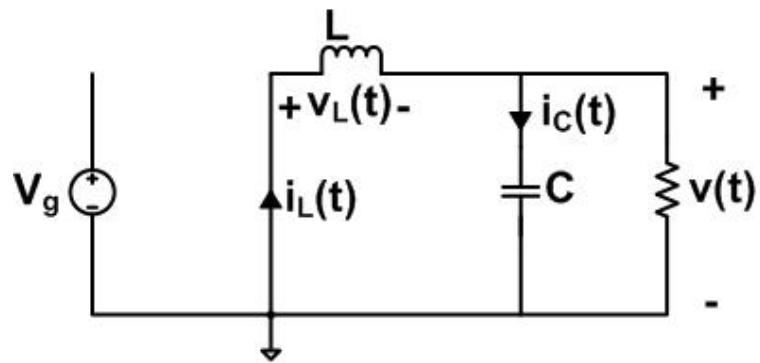
$$\|v_{\text{ripple}}(t)\| \ll V \quad \longrightarrow \quad v(t) \approx V$$

2.4 Inductive DC-DC Converter

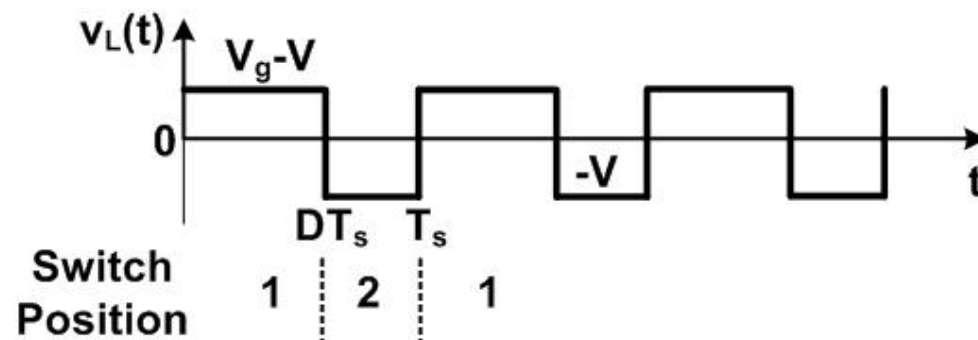
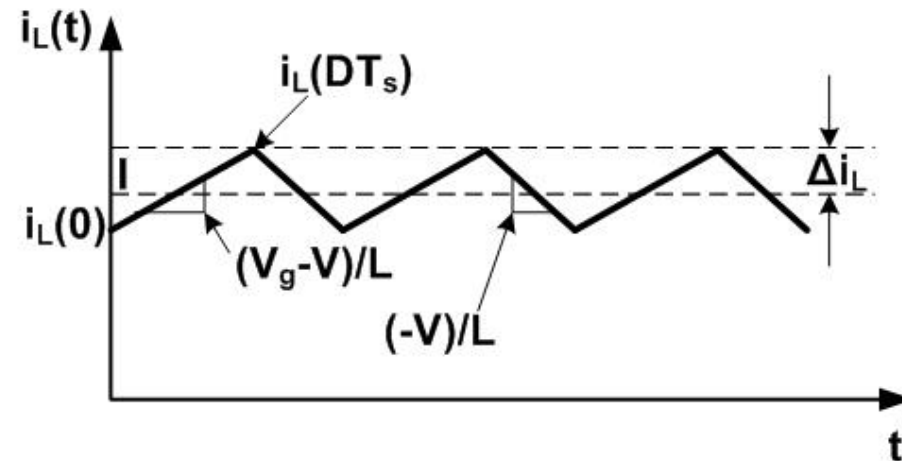
Buck Converter: Steady-State Waveforms



Position 1

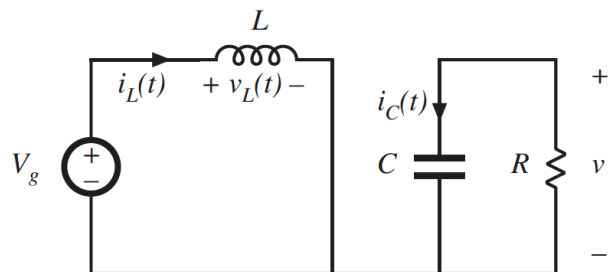
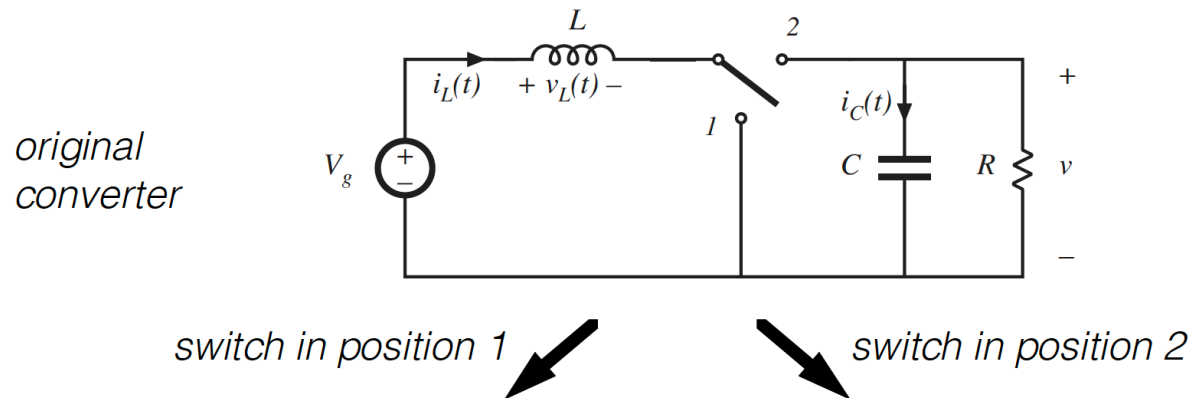


Position 2



2.4 Inductive DC-DC Converter

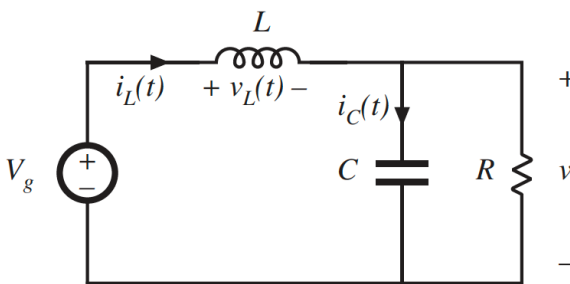
Boost Converter



$$v_L = V_g$$

$$i_C = -v / R$$

$$v(t) \approx V$$



$$v_L = V_g - v$$

$$i_C = i_L - v / R$$

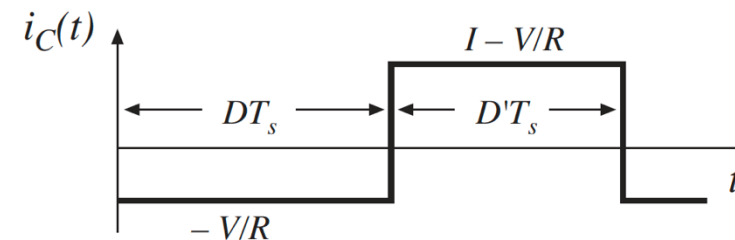
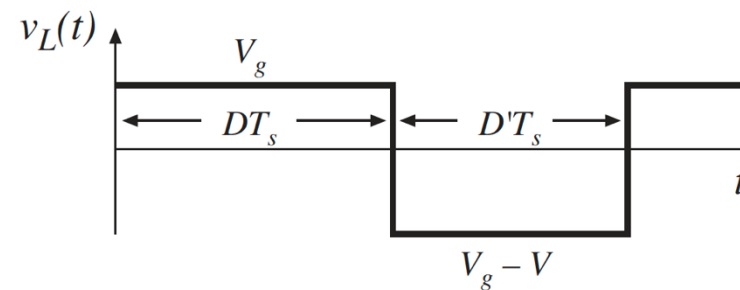
$$v(t) \approx V, \quad i_L(t) \approx I$$

$$v_L(t) = L \frac{di_L(t)}{dt}$$

$$i_L(T_s) - i_L(0) = \frac{1}{L} \int_0^{T_s} v_L(t) dt \quad \text{Zero in steady state}$$

$$\int_0^{T_s} v_L(t) dt = (V_g) DT_s + (V_g - V) D'T_s$$

$$V = \frac{V_g}{D'}$$

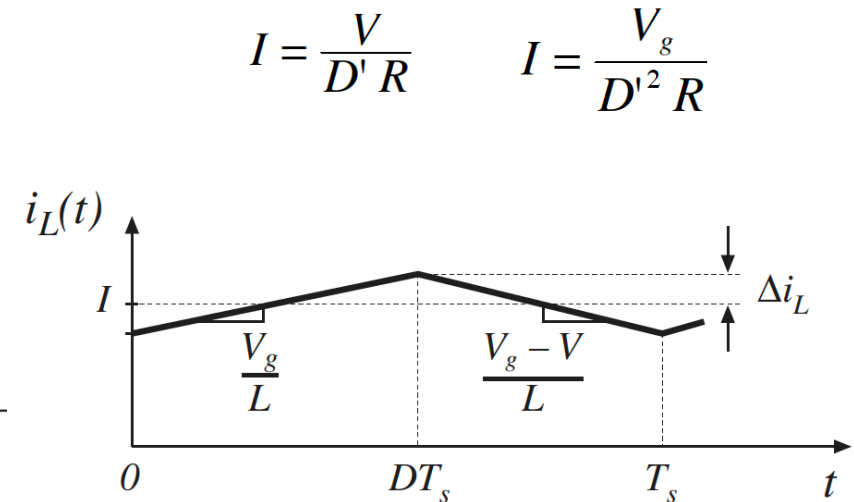
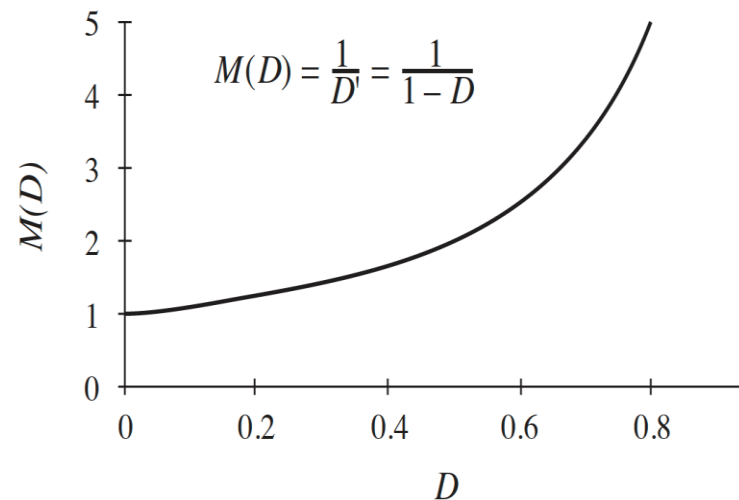


2.4 Inductive DC-DC Converter

Boost Converter

- The voltage conversion ratio, $M(D)$, is the ratio of the output to the input voltage of a DC-DC converter
- For a boost converter, the voltage conversion ratio is

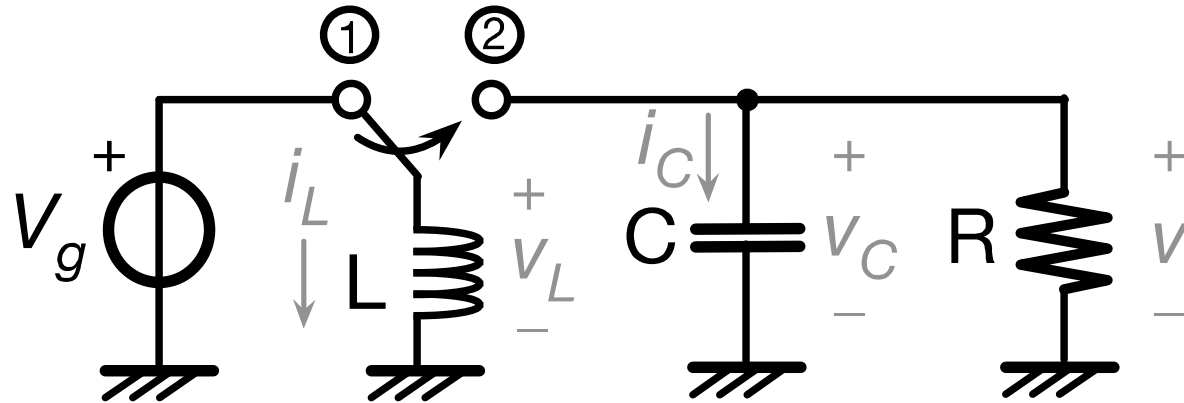
$$M(D) = \frac{V}{V_g} = \frac{1}{D'} = \frac{1}{1-D}$$



- **The inductor current**, which coincides with the DC input current in a boost converter, **is larger than the load current** and increases as D approaches 1

2.4 Inductive DC-DC Converter

Inverting Boost Converter

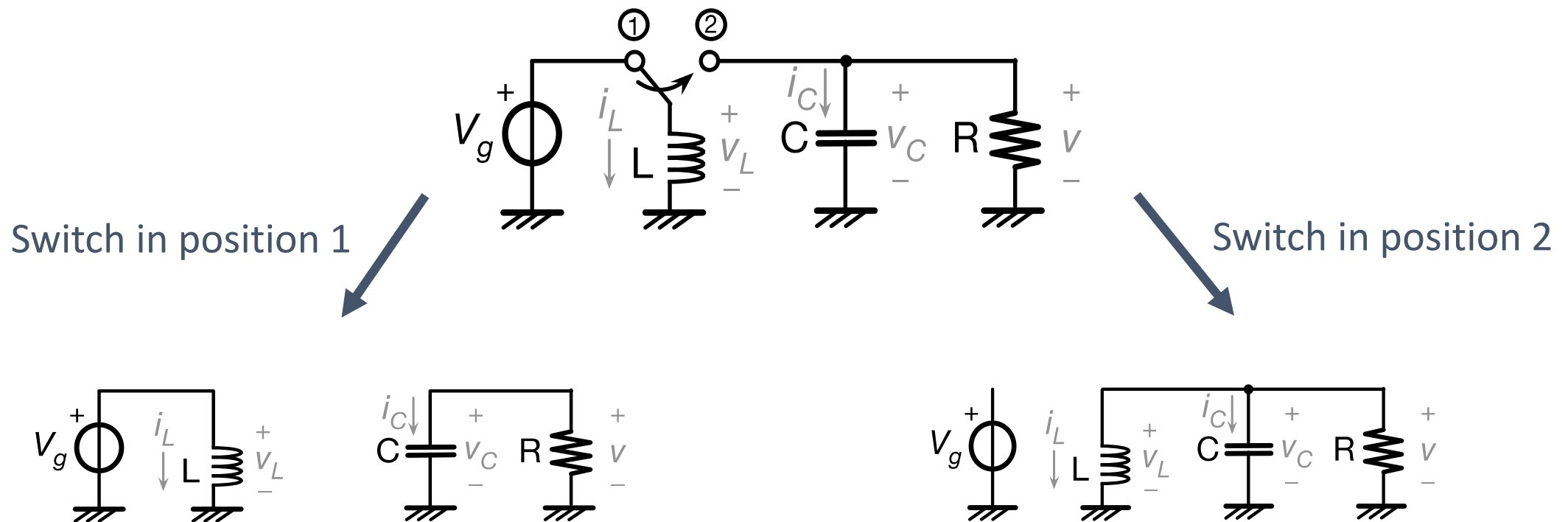


- This converter can either increase or decrease the magnitude of the DC voltage and invert its polarity
- The switch can be implemented with transistors, paying attention to the body biasing since the output voltage is negative
- This topology can be useful in AMOLED display driving

2.4 Inductive DC-DC Converter

Inverting Buck-Boost Converter

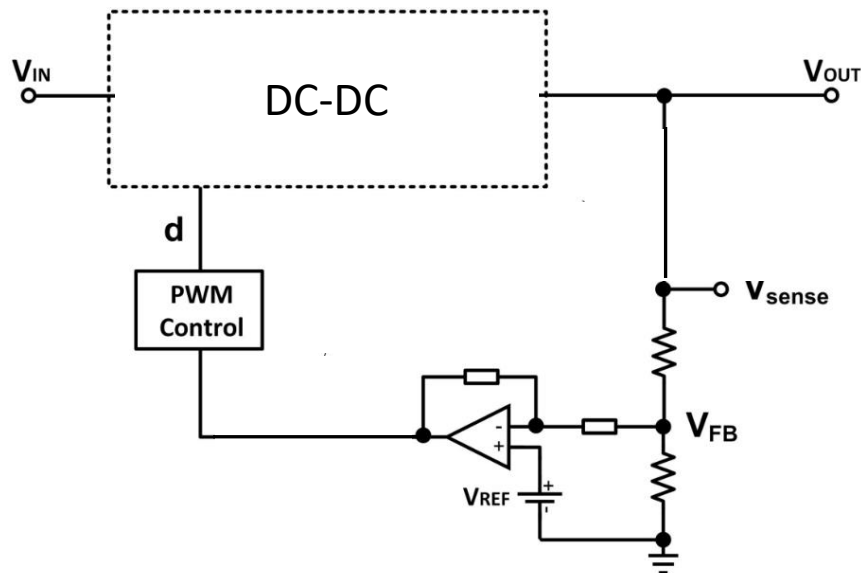
- With small-ripple approximation, and the principles of inductor volt-second balance and capacitor charge balance, we will find the steady-state output voltage and inductor current



2.4 Inductive DC-DC Converter

Closed loop Control

The desired output voltage can be set with a control in feedback loop



The control performances of the simple loop that generates the duty cycle are not satisfactory under some large disturbance signals [1-4]

1. Proportional integral derivative (PID) control methods [5-6]
2. nonlinear controller designs for DC-DC converters [7-9]
3. Sliding mode control [10-12]
4. neural network [13-14]
5. intelligent control

2.4 Inductive DC-DC Converter

Switching controllers

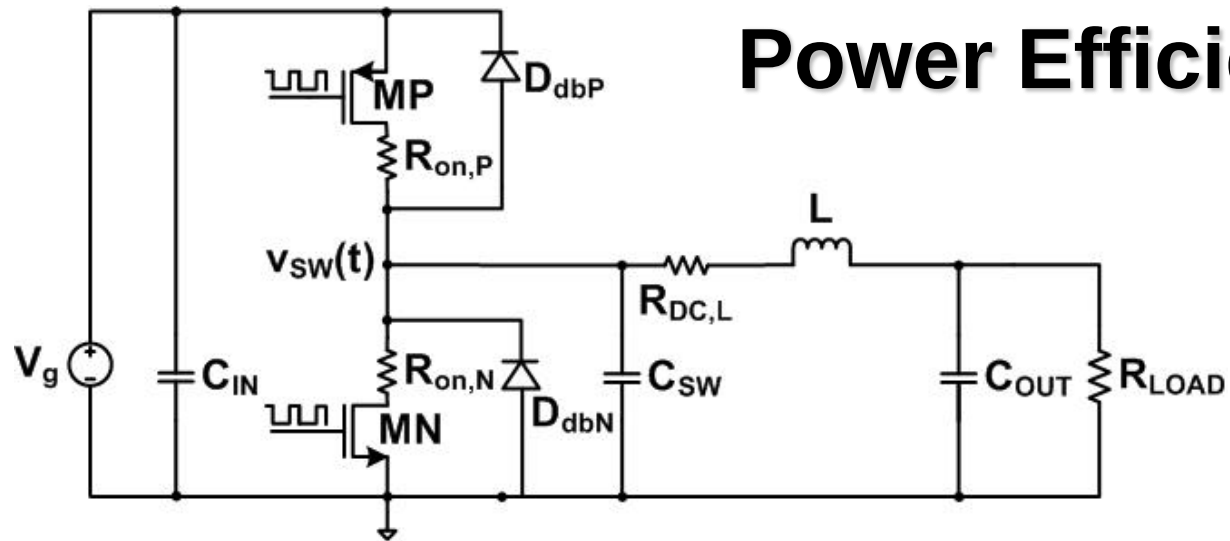
In any switching regulator, a controller is needed to regulate the output voltage by changing the switching activity. The approaches are :

PWM (Pulse width modulation) : The duty cycle between input/output switches is modified. Advantages : fixed frequency. Drawbacks : high switching losses when the load is light

PFM (Pulse Frequency Modulation) : pulses with same duration are used, but their repetition rate is changed. Advantages : losses scale with load current. Drawback : very varying frequency, unpredictable harmonic noise.

Burst mode : The regulator is clocked only when the output voltage drops below a given threshold, reducing by 95 % the converter quiescent power.

2.4 Inductive DC-DC Converter



Power Efficiency

$$\eta = \frac{\text{Output DC Power}}{\text{Input DC Power}} = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{loss}}}$$

- ❑ **DC losses** → conduction losses and quiescent current → heavy-load issues
 - Metal traces parasitic resistance
 - Power switches on-resistance
 - Inductor-winding resistance
 - Control circuit bias current
- ❑ **AC losses** → switching losses → light-load issues
 - Capacitive-driver loss
 - Dead-time parasitic diode loss

2.4 Inductive DC-DC Converter

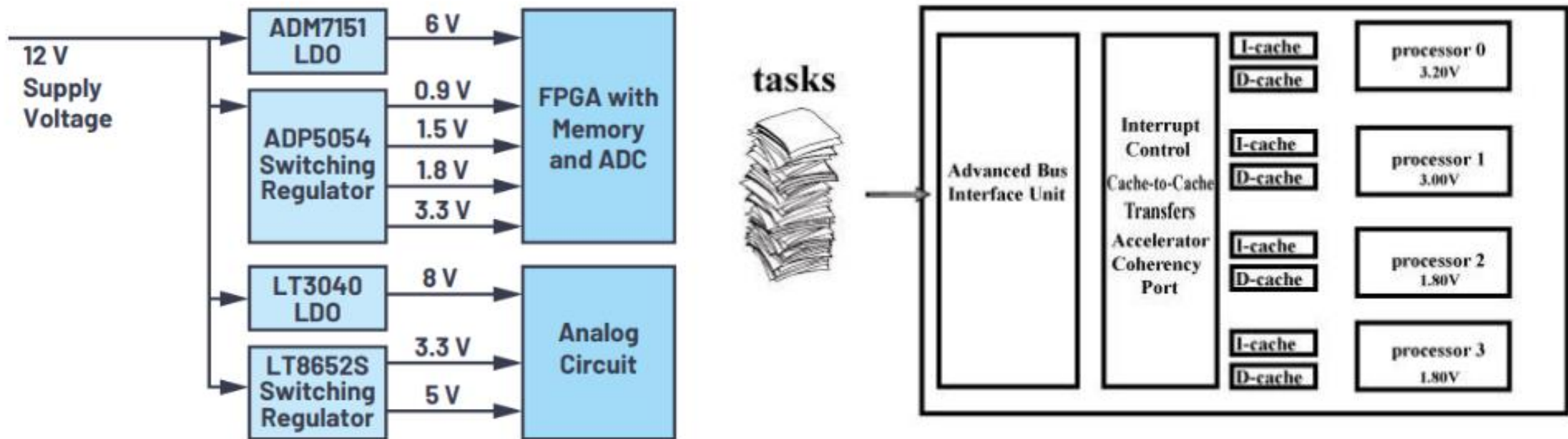
References Closed Loop Control

1. Chen, J.J.; Hsu, J.H.; Hwang, Y.S.; Yu, C.C.; A DC-DC buck converter with load-regulation improvement using dual-path-feedback techniques. *Analog. Integr. Circuits Signal Proc.* 2014, 79, 149–159.
2. Ding, S.H.; Zheng, W.X.; Sun, J.; Wang, J. Second-order sliding mode controller design and its implementation for buck converters. *IEEE Trans. Ind. Inf.* 2018, 14, 1990–2000.
3. Shabestari, P.M.; Gharehpetian, G.B.; Riahy, G.H.; Mortazavian, S.; Voltage controllers for DC-DC boost converters in discontinuous current mode. In *IESC*, NY, USA, November 2015; pp. 1–7.
4. Kancherla, S.; Tripathi, R.K.; Nonlinear average current mode control for a DC-DC Buck converter In *Proceedings of the IEEE Inter. Conference on Sustainable Energy Tech.*, 2008; pp. 831–836.
5. Tan, S.C.; Lai, Y.M.; Cheung, M.K.H.; Tse, C.K. On the practical design of a sliding mode voltage controlled buck converter. *IEEE Trans. Power Electron.* 2005, 20, 425–437.
6. Zhang, Y.; Zhang, B.; Chen, B.; Hu, Z. A; Novel Control Law of Boost DC-DC Converter Based on Bilinear Theory. *Trans. China Electrotech. Soc.* 2006, 21, 109–114.
7. Tan, S.C.; Lai, Y.M.; Chi, K.T. General Design Issues of Sliding-Mode Controllers in DC-DC Converters. *IEEE Trans. Ind. Electron.* 2008, 55, 1160–1174.
8. Ni, Y.; Xu, J.P.; Design of a novel discrete global sliding mode controlled Buck converter. *Electr. Mach. Control* 2009, 23, 112–116.
9. Komurcugil, H.; Non-singular terminal sliding-mode control of DC-DC buck converters. *Control Eng. Pract.* 2013, 21, 321–332.
10. Delgado, F.; Magana, M.E.; A fuzzy logic controller design and simulation for a sawmill bucking system. *IEEE Trans. Ind. Electron.* 2005, 52, 628–634.
11. Alrabadi, A.N.; Barghash, M.A.; Abuzeid, O.M.; Intelligent Regulation Using Genetic Algorithm-Based Tuning for the Fuzzy Control of the Power Electronic Switching-Mode Buck Converter. Available online.
12. Saravanan, A.G.; Rajaram, M.; Fuzzy controller for dynamic performance improvement of a half-bridge isolated dc-dc converter. *Neurocomputing* 2014, 140, 283–290.
13. Piazza, M.C.D.; Pucci, M.; Ragusa, A.; Vitale, G.; Analytical versus neural real-time simulation of a photovoltaic generator based on a DC-DC converter. *IEEE Trans. Ind. Appl.* 2010, 46, 2501–2510.
14. Bingöl, O.; Pacaci, S.; A Virtual Laboratory for Neural Network Controlled DC Motors Based on a DC-DC Buck Converter. *Int. J. Eng. Educ.* 2012, 28, 713–723.

2.5 SIMO and SIDO DC-DC Converter

Complex systems can include parts that operate with different supply voltages

Analog
Memories
Digital

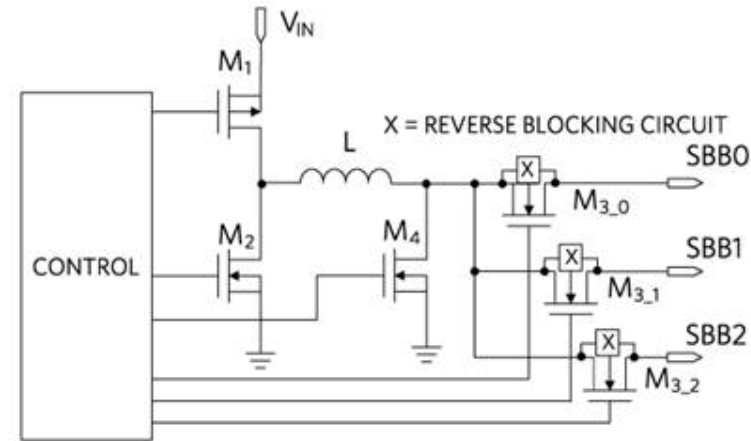
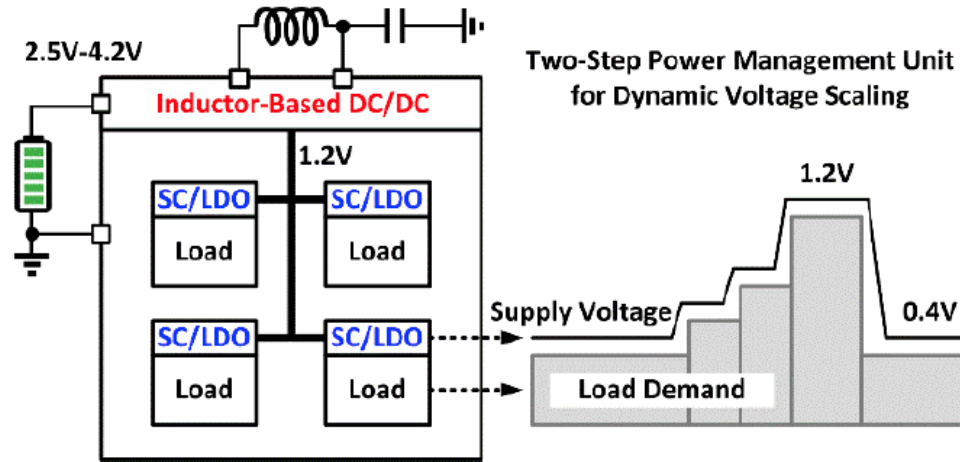
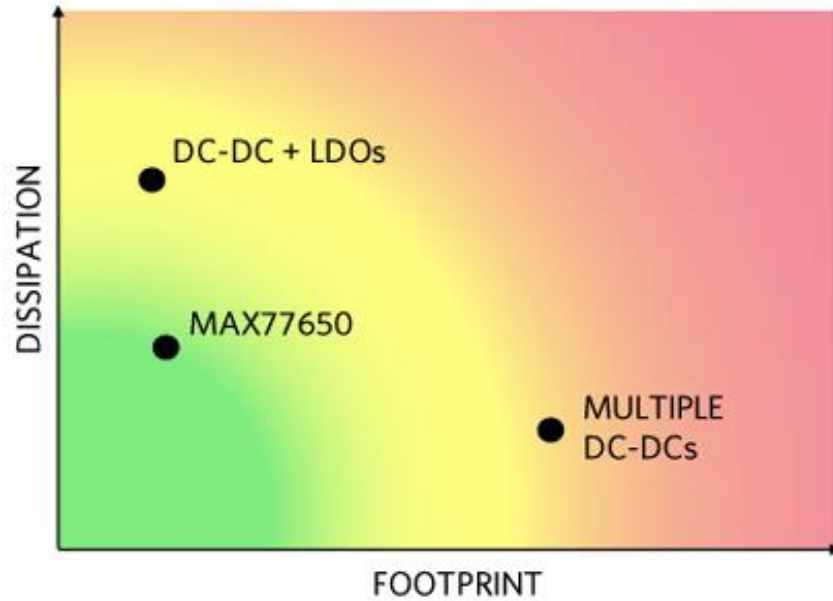


2.5 SIMO and SIDO DC-DC Converter

Power Management for Complex Systems

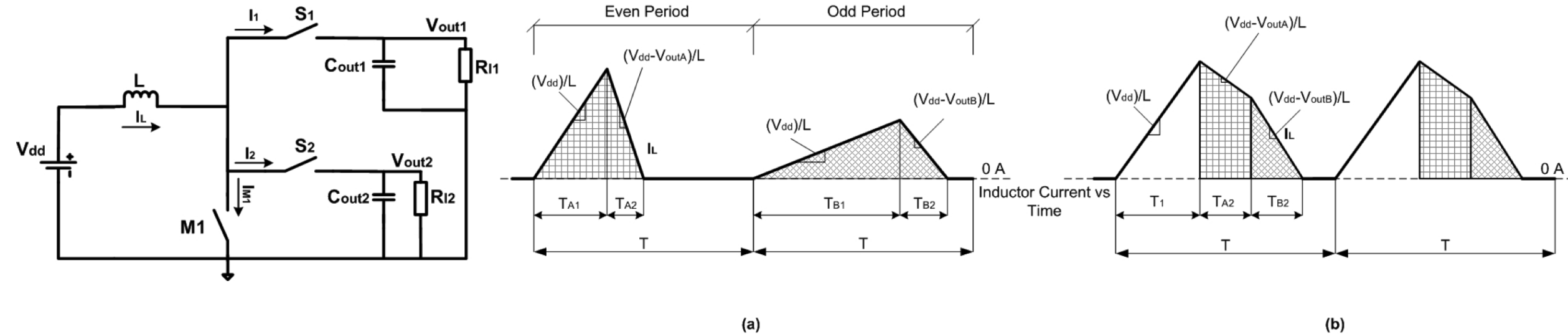
Possible Strategies

- Multiple DC-DC converters
- Inductor based plus LDO
- Single Inductor Multiple Output SIMO



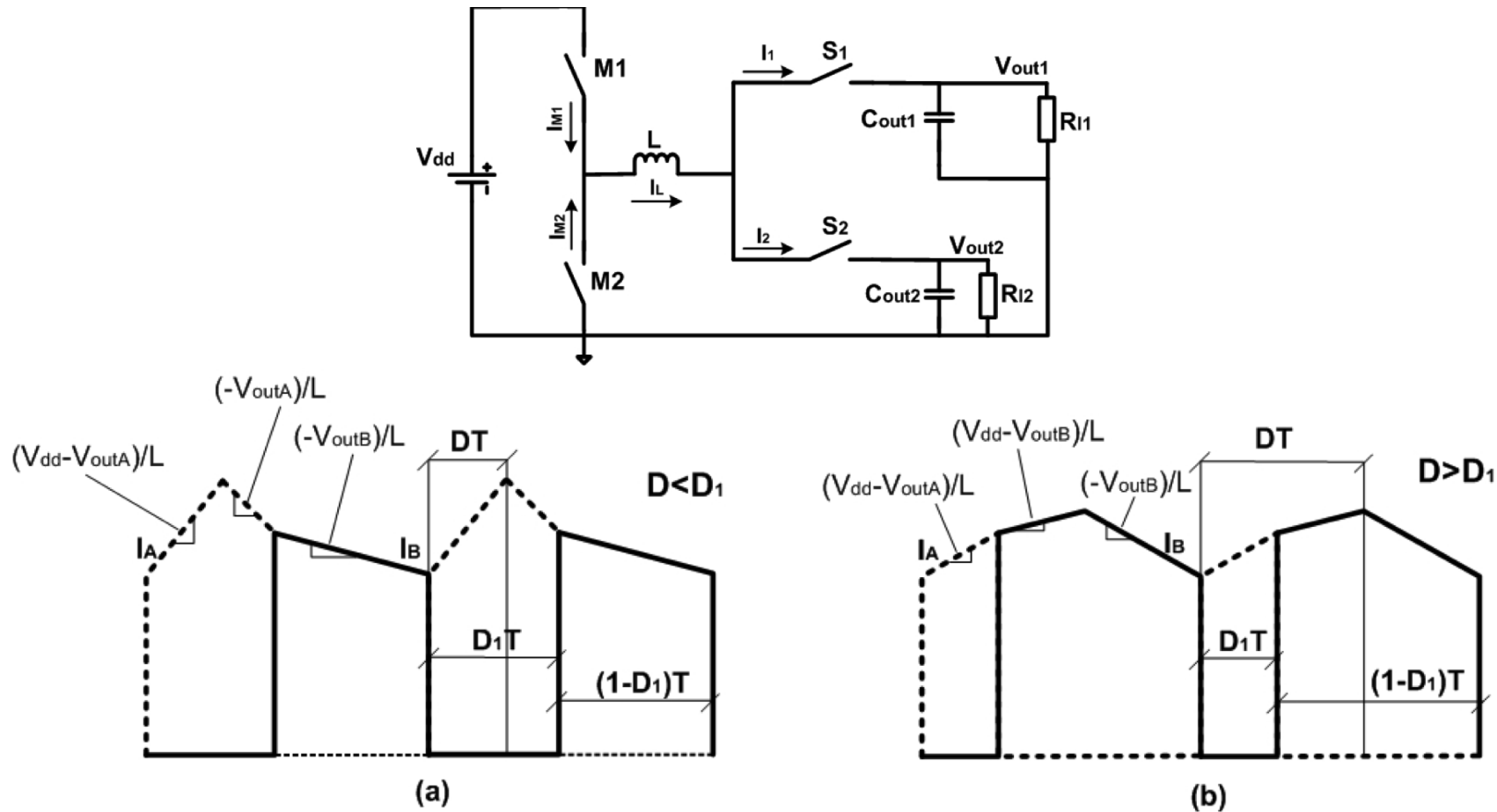
2.5 SIMO and SIDO DC-DC Converter

- Inductor based DC-DC converters achieve a good efficiency and low ripple
- The main limit is the bulky inductance
- Solution is to increase the sampling frequency but the dynamic power consumption increases.
- The problem is augmented when multiple supply voltages are required.
- Use of Single Inductor double or multiple output (SIDO or SIMO)



2.4 SIMO and SIDO DC-DC Converter

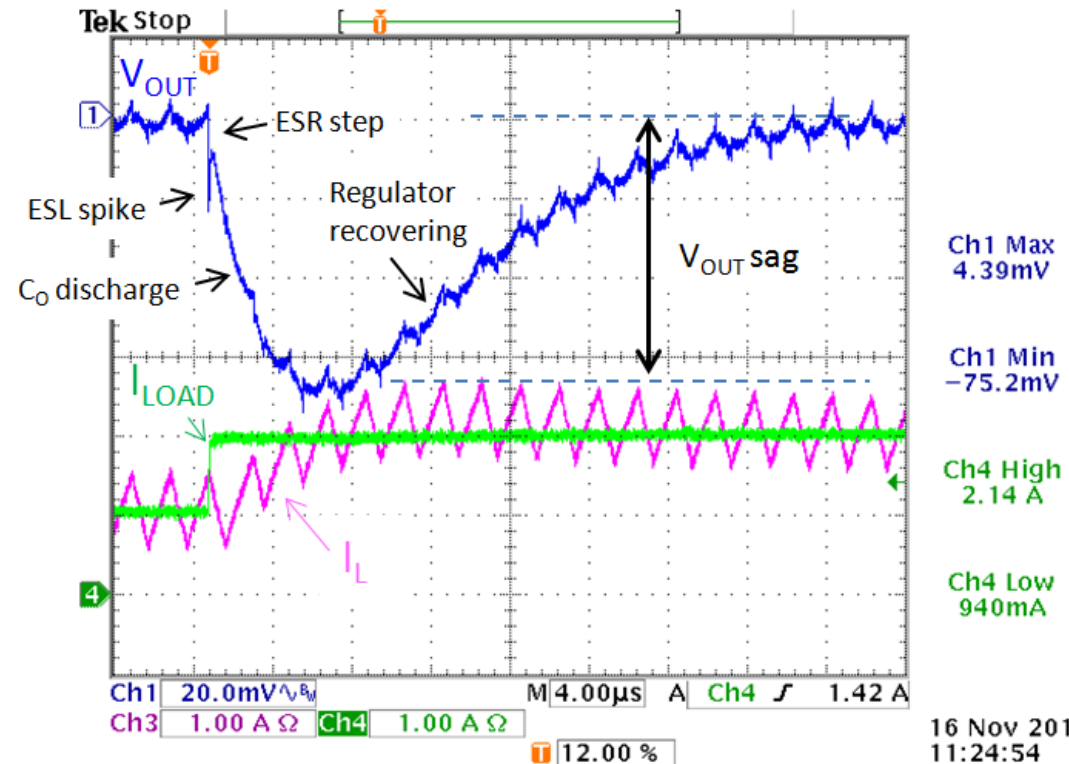
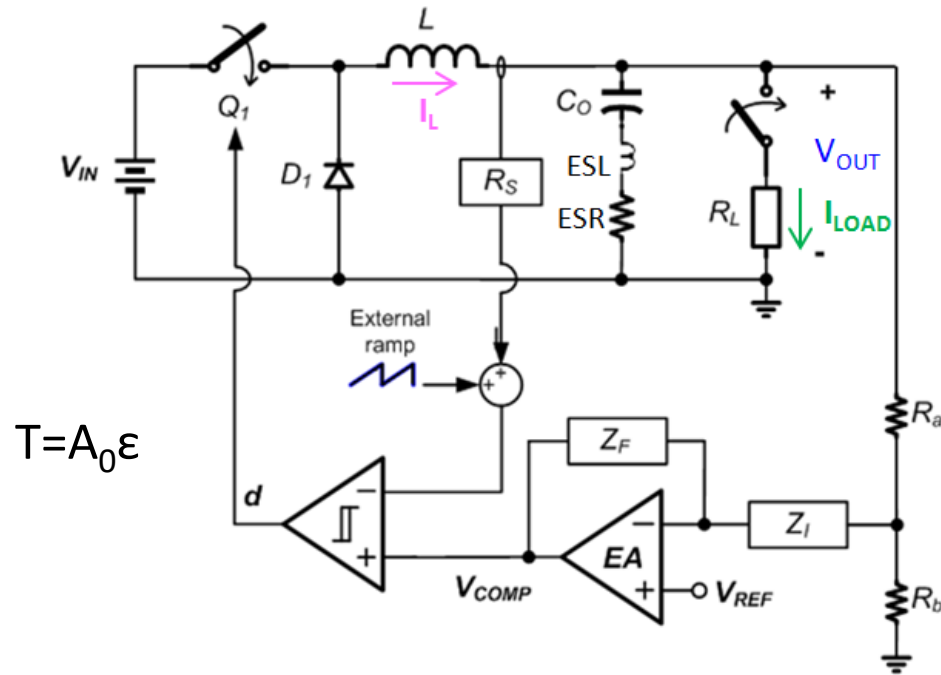
- Buck converter with two outputs



Needs extra switches

2.4 SIMO and SIDO DC-DC Converter

- Single output Control

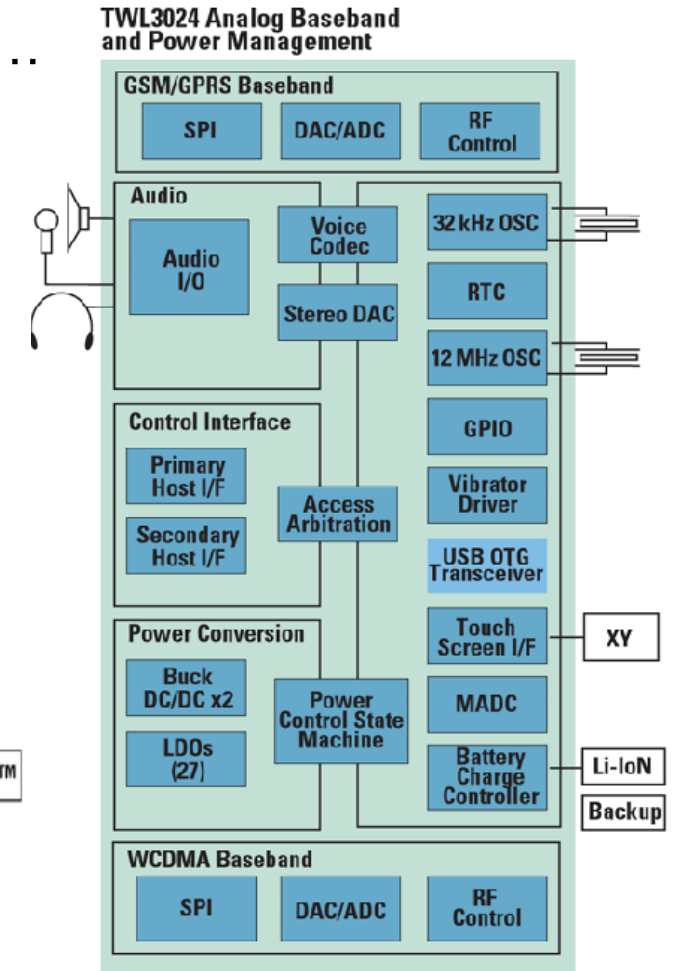
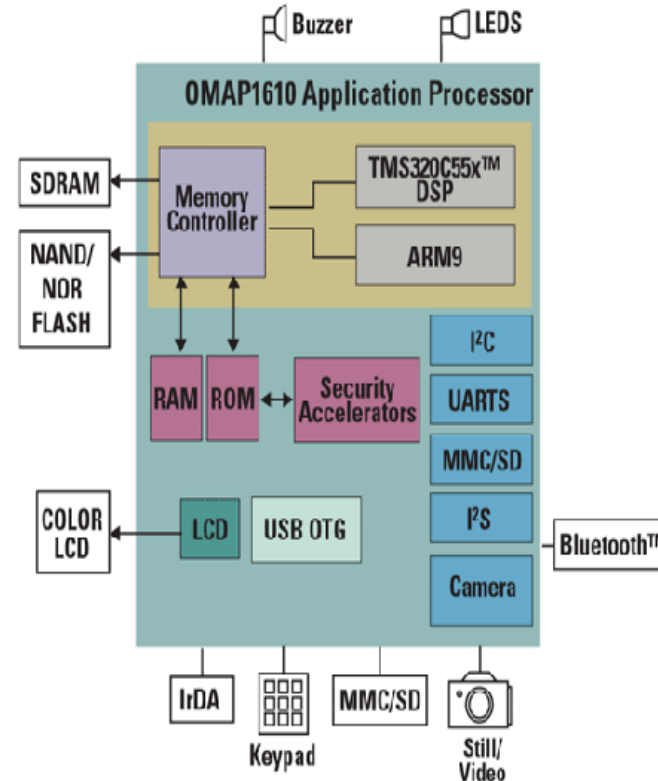


- Multiple output control
- Pragmatic approach (look at the goal)
- Analytical approach (try to use control theory)

2.5 SIMO and SIDO DC-DC Converter

Application Example: Pragmatic approach

- Power management modules integrated with digital processor, memory, ...
- Challenges : integration in sub-micron technology ($0.13\mu\text{m}$)
- Power management must provides: Regulation Supply, Noise Isolation, Battery Monitor, Drivers

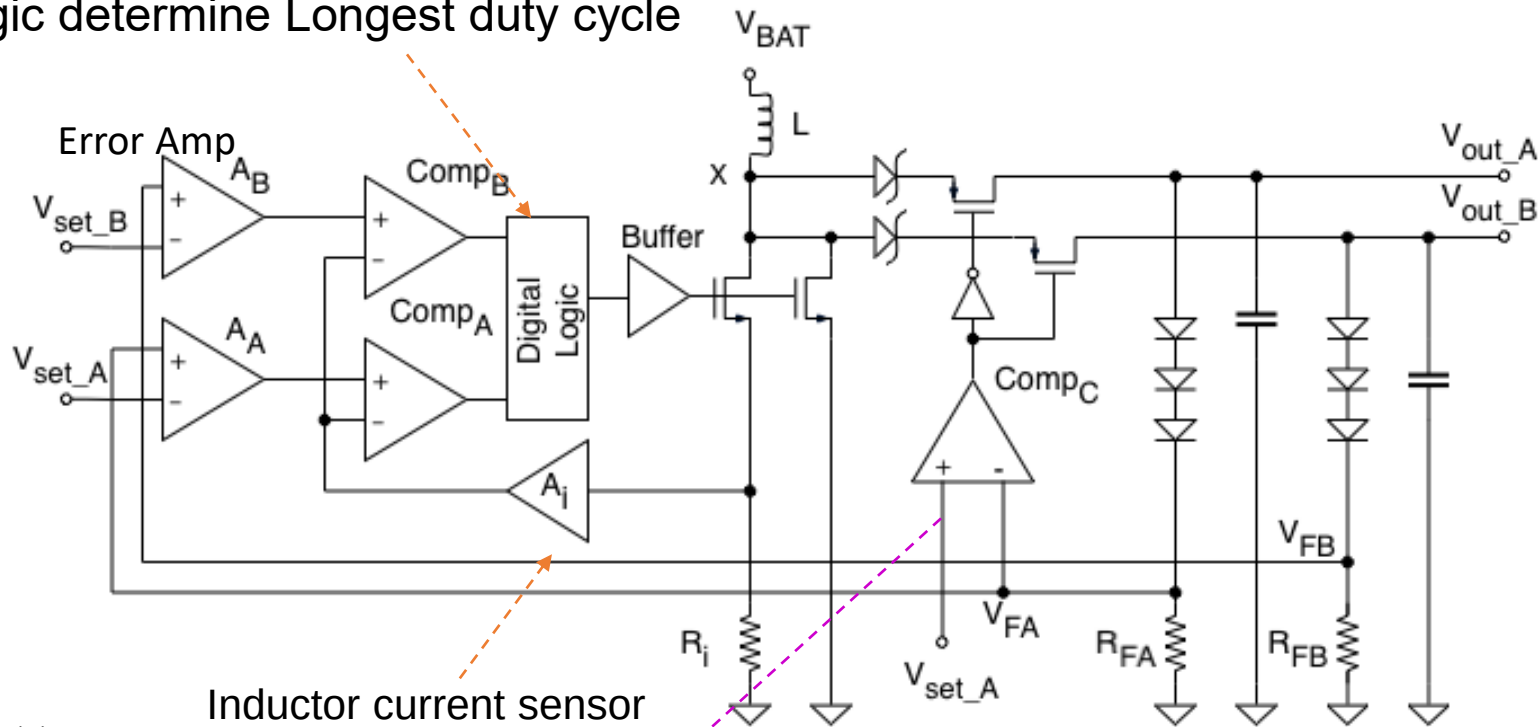


Supply of white LEDs in cell phones

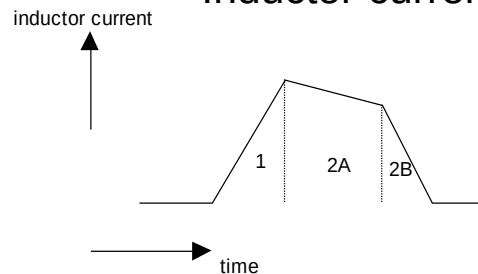
2.5 SIMO and SIDO DC-DC Converter

Designed System

Logic determine Longest duty cycle



Inductor current sensor



S.K. Hoon, N. Culp, J. Chen, F. Maloberti: "A PWM Dual-Output DC/DC Boost Converter in a 0.13 μ m CMOS Technology for Cellular-Phone Backlight Application"; ESSCIRC 2005, pp. 81-84.

2.5 SIMO and SIDO DC-DC Converter

4 Output Control: Analytical approach

- Main duty:

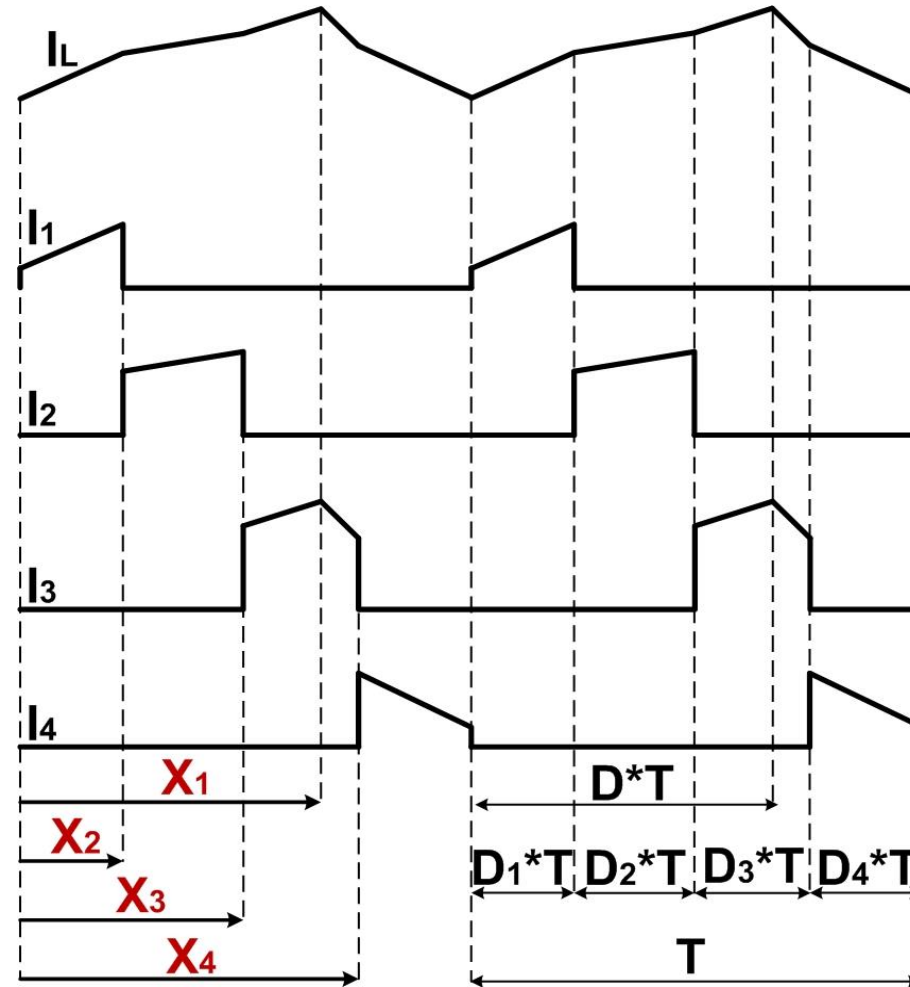
$$D = \frac{T_{on,MP}}{T}$$

- Sharing Duties:

$$D_i = \frac{T_{on,SW_i}}{T}$$

- The controller must determine the times:

X_1, X_2, X_3, X_4



2.5 SIMO and SIDO DC-DC Converter

❑ Multiple output Control

$$\begin{cases} T_1 = a_{11}\varepsilon_1 + a_{12}\varepsilon_2 + \dots + a_{1N}\varepsilon_N \\ T_2 = a_{21}\varepsilon_1 + a_{22}\varepsilon_2 + \dots + a_{2N}\varepsilon_N \\ \dots \\ T_N = a_{N1}\varepsilon_1 + a_{N2}\varepsilon_2 + \dots + a_{NN}\varepsilon_N \end{cases}$$

$$\mathbf{T} = k\mathbf{A}\mathbf{E}$$

- ❑ K is the loop gain; if k is large the time vector is determined by a negligible error vector

M. Belloni, E. Bonizzoni, E. Kiseliovas, P. Malcovati, F. Maloberti, T. Peltola, T. Teppo: "A 4-Output Single-Inductor DC-DC Buck Converter with Self-Boosted Switch Drivers and 1.2A Total Output Current" ISSCC 2008.

2.5 SIMO and SIDO DC-DC Converter

- ❑ How to choose the matrix **A**?
- ❑ Many possibilities: diagonal or more complex
 - ➡ Trade off stability, accuracy, complexity
 - ➡ For boost remember the constrain $T_1 > T_2, \dots, T_N$

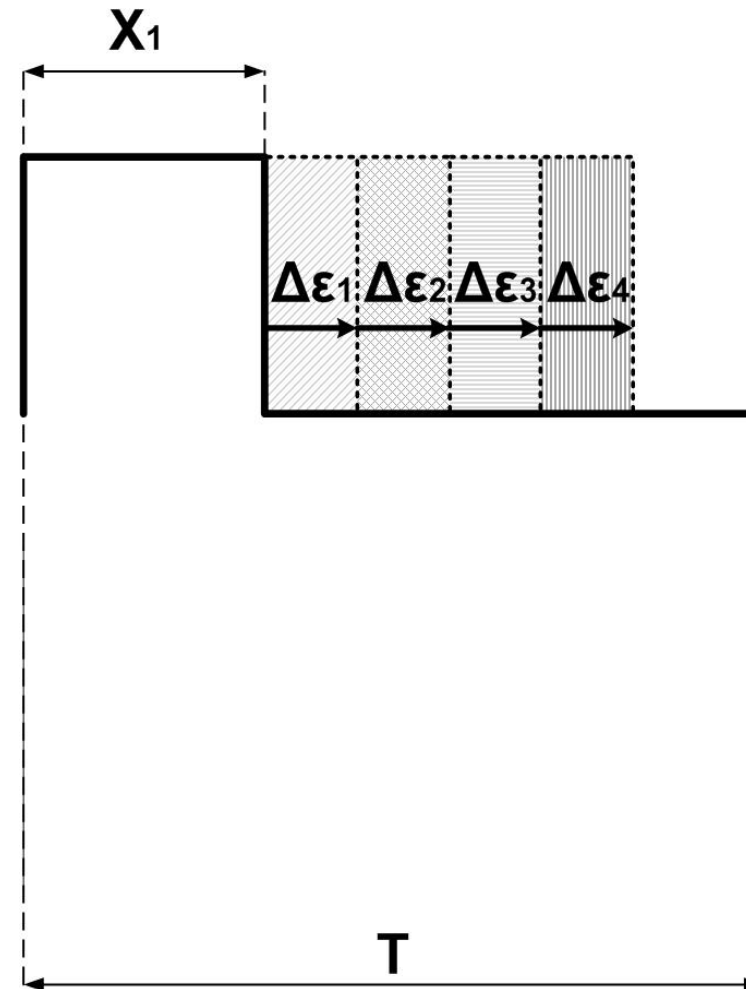
$$A = \begin{bmatrix} 1 & 0 & \dots & 0 & 0 \\ 0 & 1 & \dots & 0 & 0 \\ 0 & 0 & \dots & 0 & 0 \\ 0 & 0 & \dots & 1 & 0 \\ 0 & 0 & \dots & 0 & 1 \end{bmatrix}$$

$$A = \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & -1 & -1 & -1 \\ 1 & 1 & -1 & -1 \\ 1 & 1 & 1 & -1 \end{bmatrix}$$

2.5 SIMO and SIDO DC-DC Converter

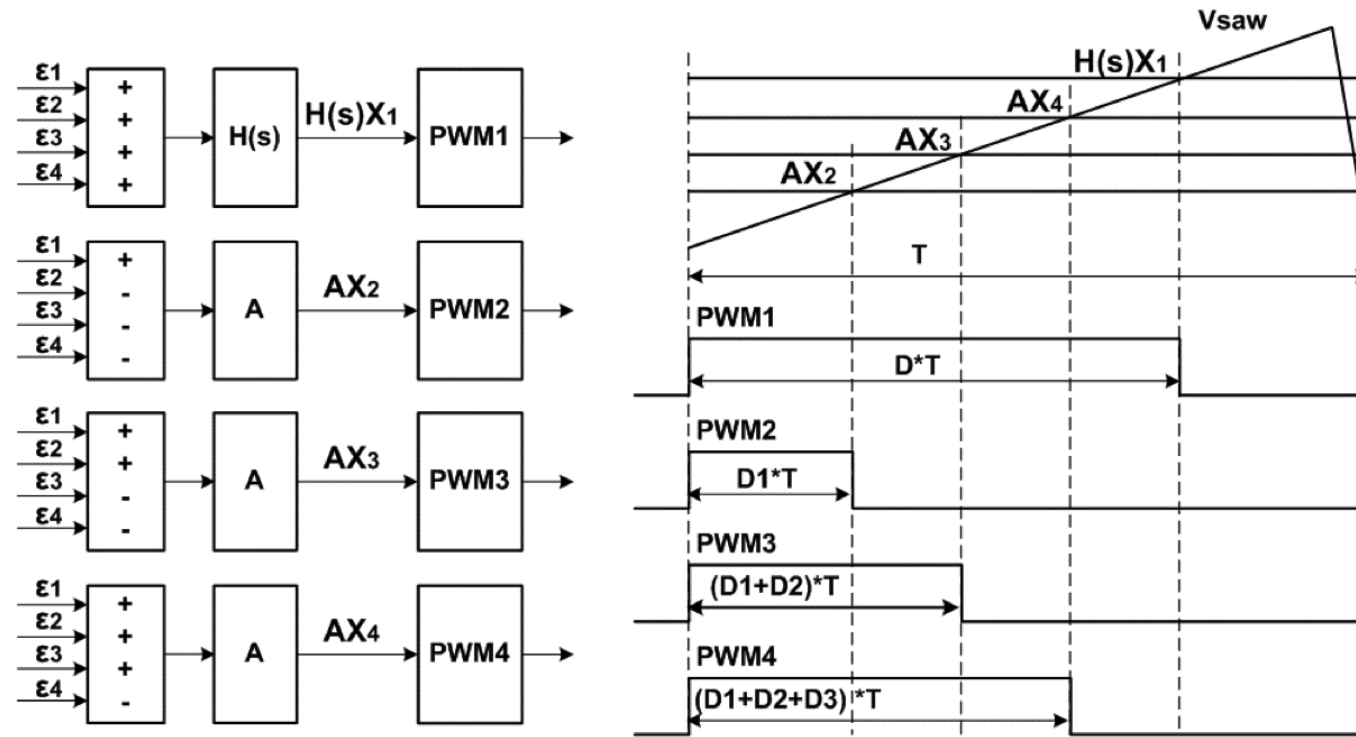
Control Strategy

- If $\Delta(\epsilon_1 + \epsilon_2 + \epsilon_3 + \epsilon_4) > 0$
 - The whole system needs more energy
 - X_1 (main) should increase
- If $\Delta(\epsilon_1 + \epsilon_2 + \epsilon_3 + \epsilon_4) < 0$
 - The whole system needs less energy
 - X_1 should decrease



2.5 SIMO and SIDO DC-DC Converter

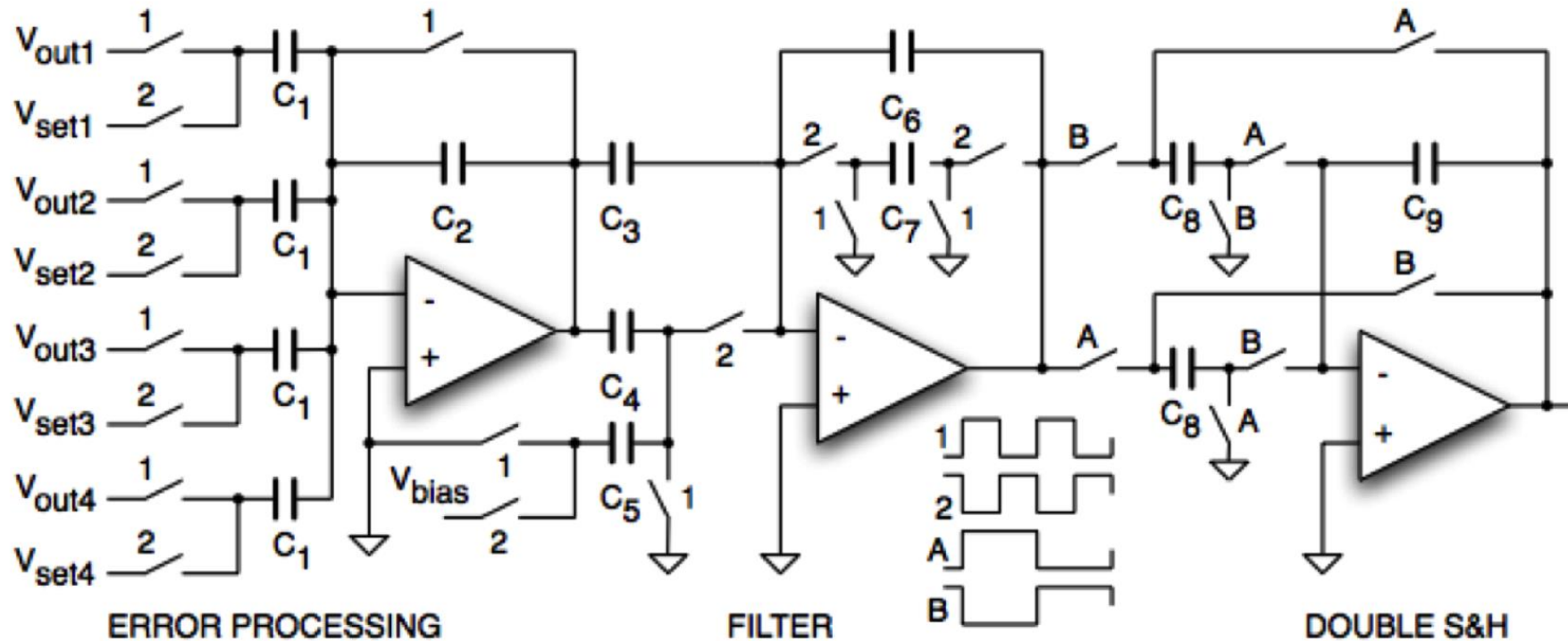
Single-Inductor 4-Output Closed-Loop Control



- $H(s) \rightarrow$ First-order zero-pole filter
- $A \rightarrow$ Gain

2.5 SIMO and SIDO DC-DC Converter

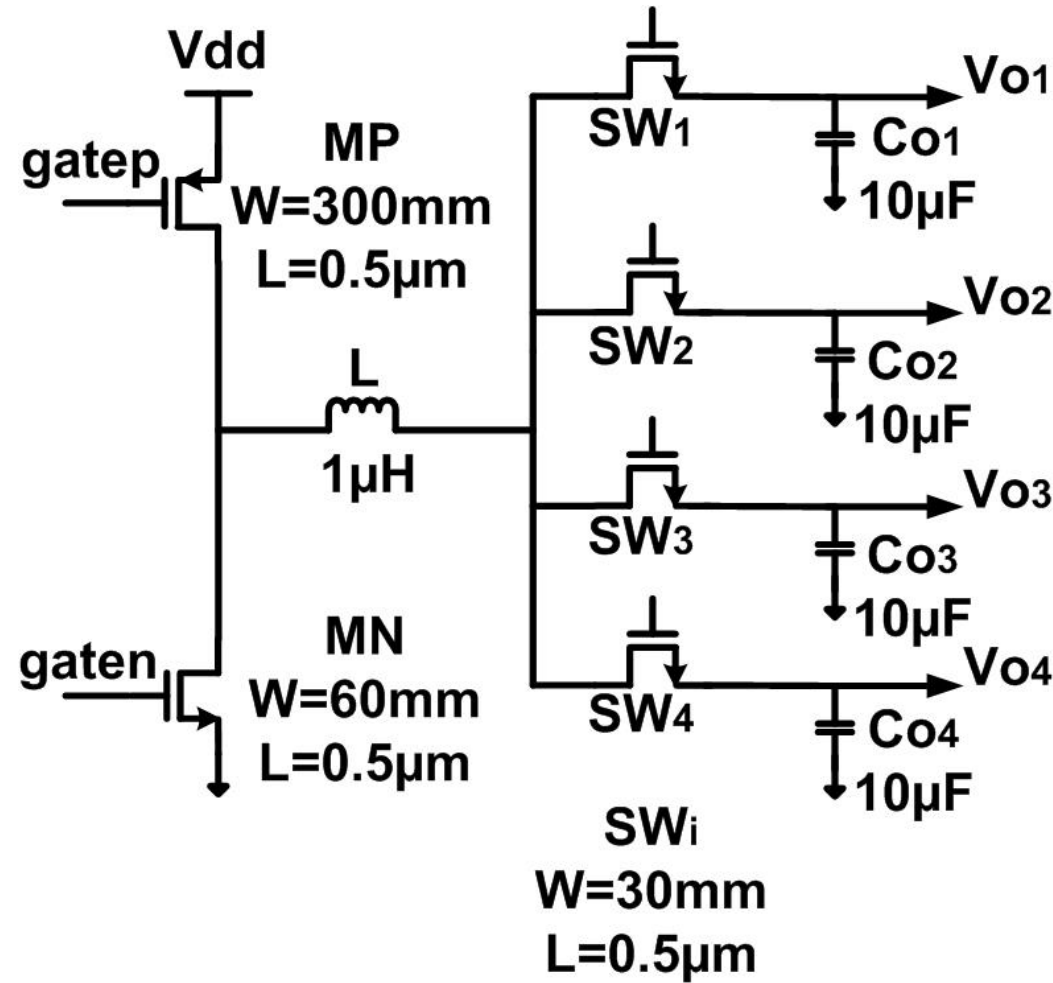
- *Analog Processing*



2.5 SIMO and SIDO DC-DC Converter

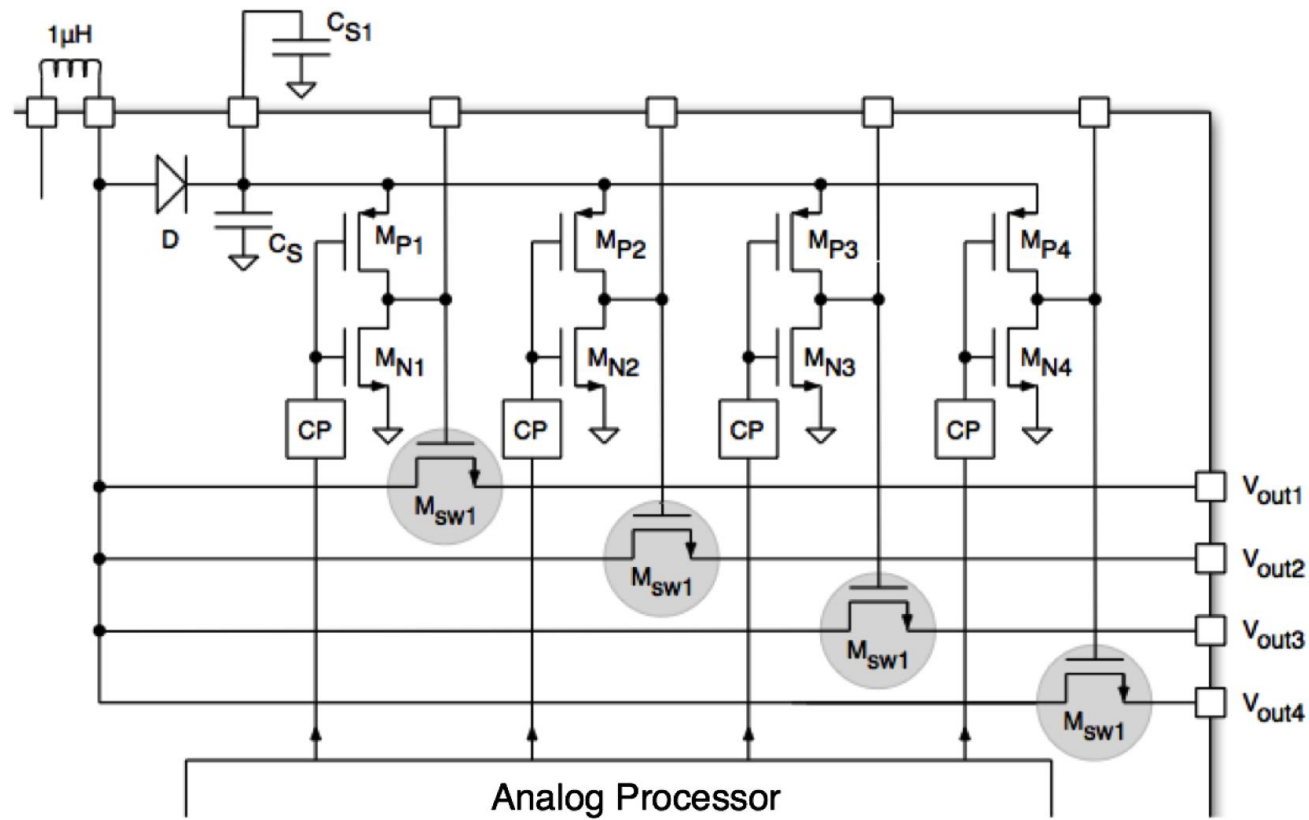
Power Stage Switch Driving Strategy

- ❑ Disoverlapped phases generator driver for p-type and n-type main-switches MP, MN
- ❑ Self-boosted snubber circuit to drive load-switches SW_i
 - Inductor current recycling during driving phases dis-overlap
 - Voltage spikes protection
 - No extra driving-power required



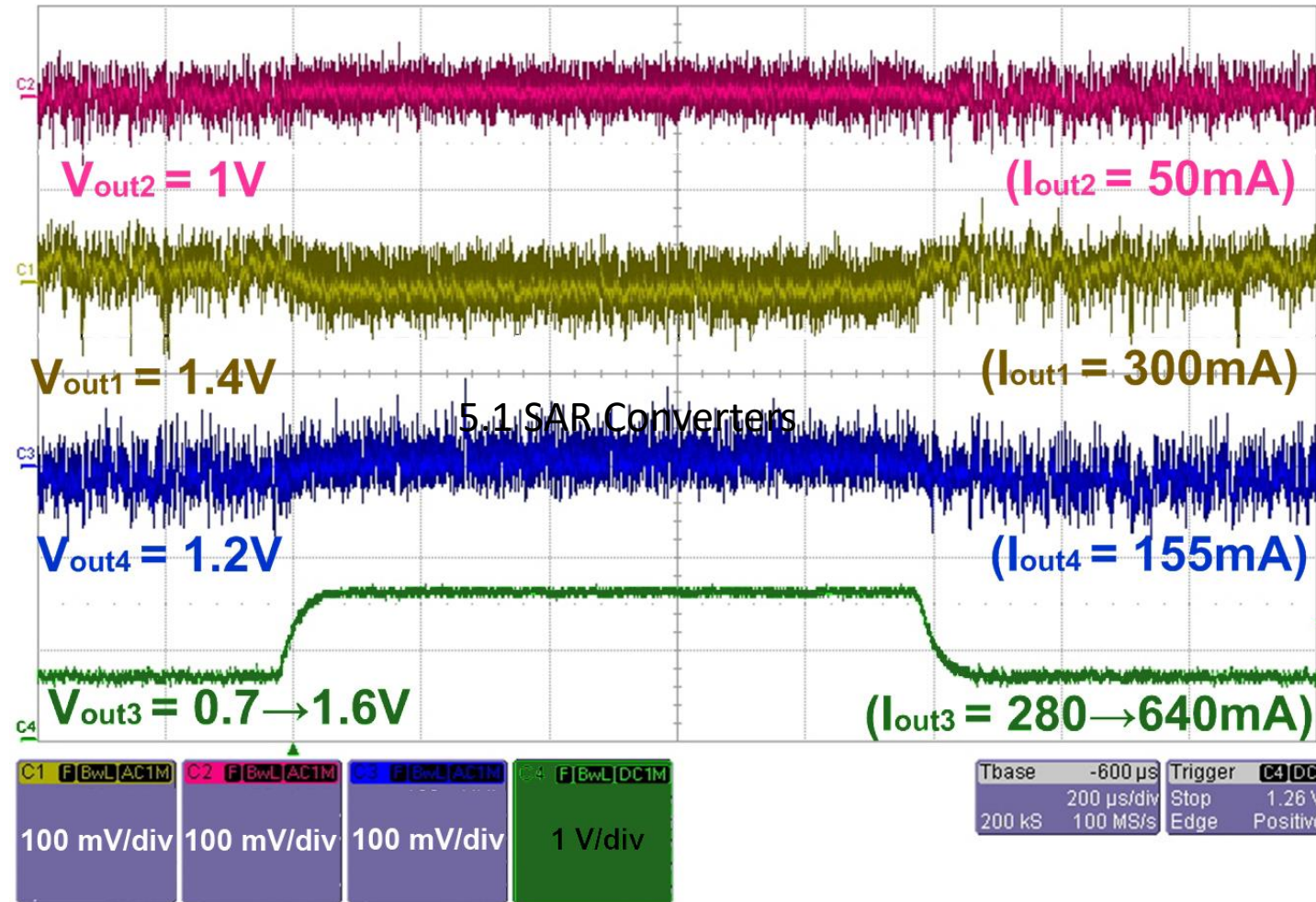
2.5 SIMO and SIDO DC-DC Converter

- *SIMO: Self boost snubber*



2.5 SIMO and SIDO DC-DC Converter

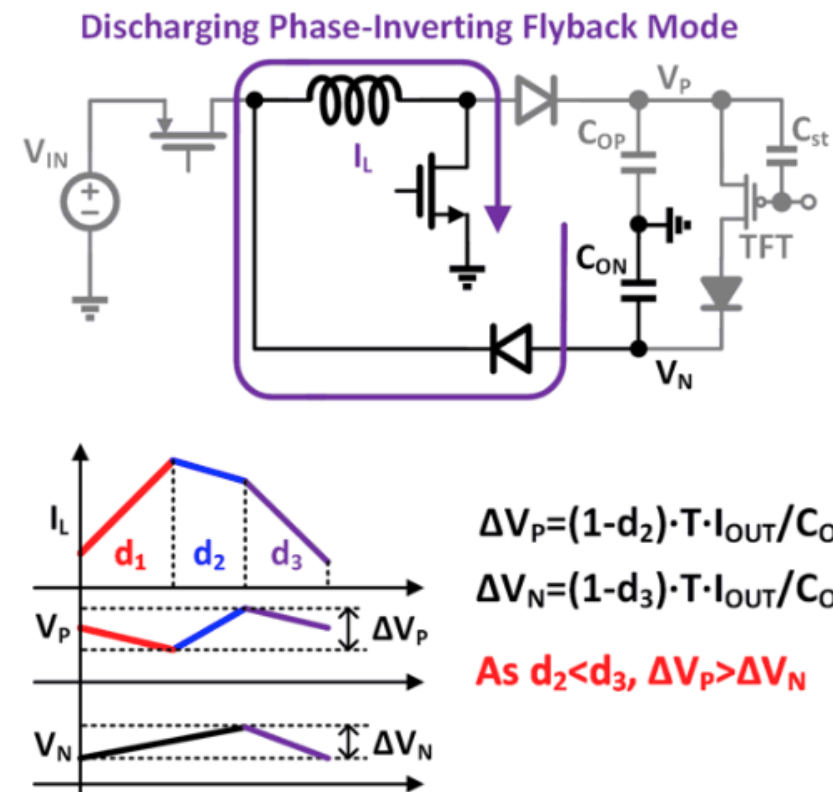
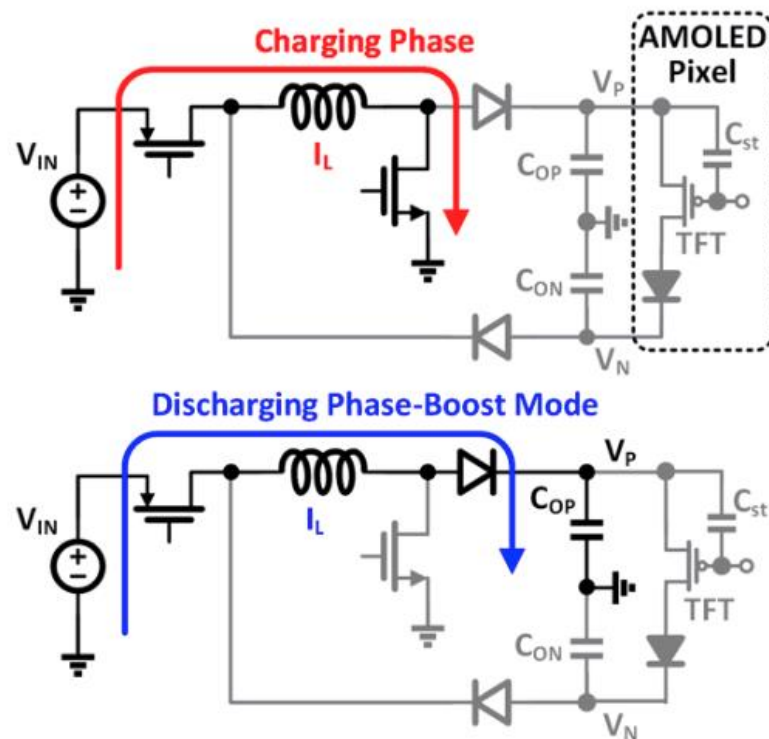
Cross Regulation



2.5 SIBO DC-DC Converter

Single Inductor Bipolar Output

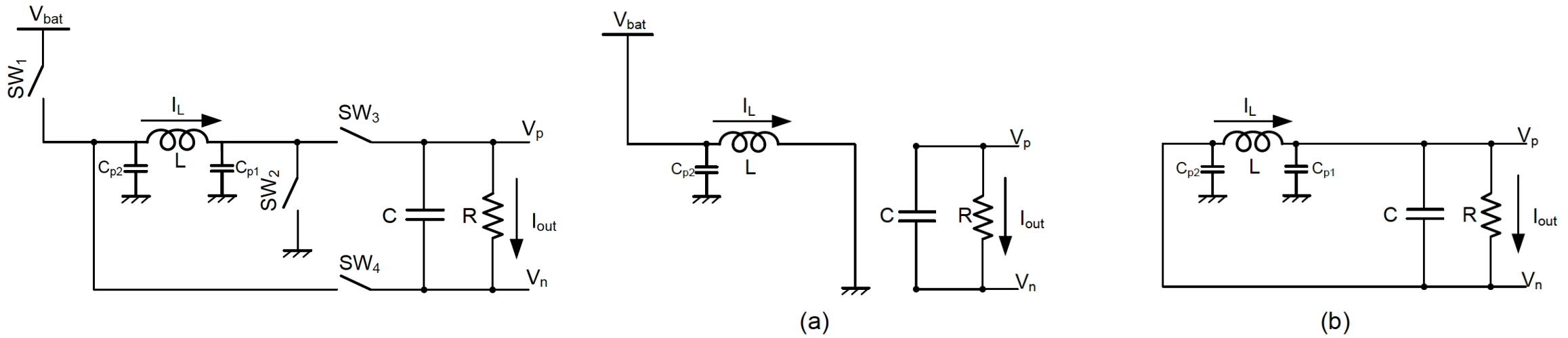
To drive the AMOLED displays, bipolar supply rails are usually required, with a fixed positive voltage supplying the current sources for pixel-level color control, and a programmable negative supply voltage controlling the display output power for brightness.



2.5 SIBO DC-DC Converter

Single Inductor Bipolar Output

Use of two phases (Master thesis F. Boera).



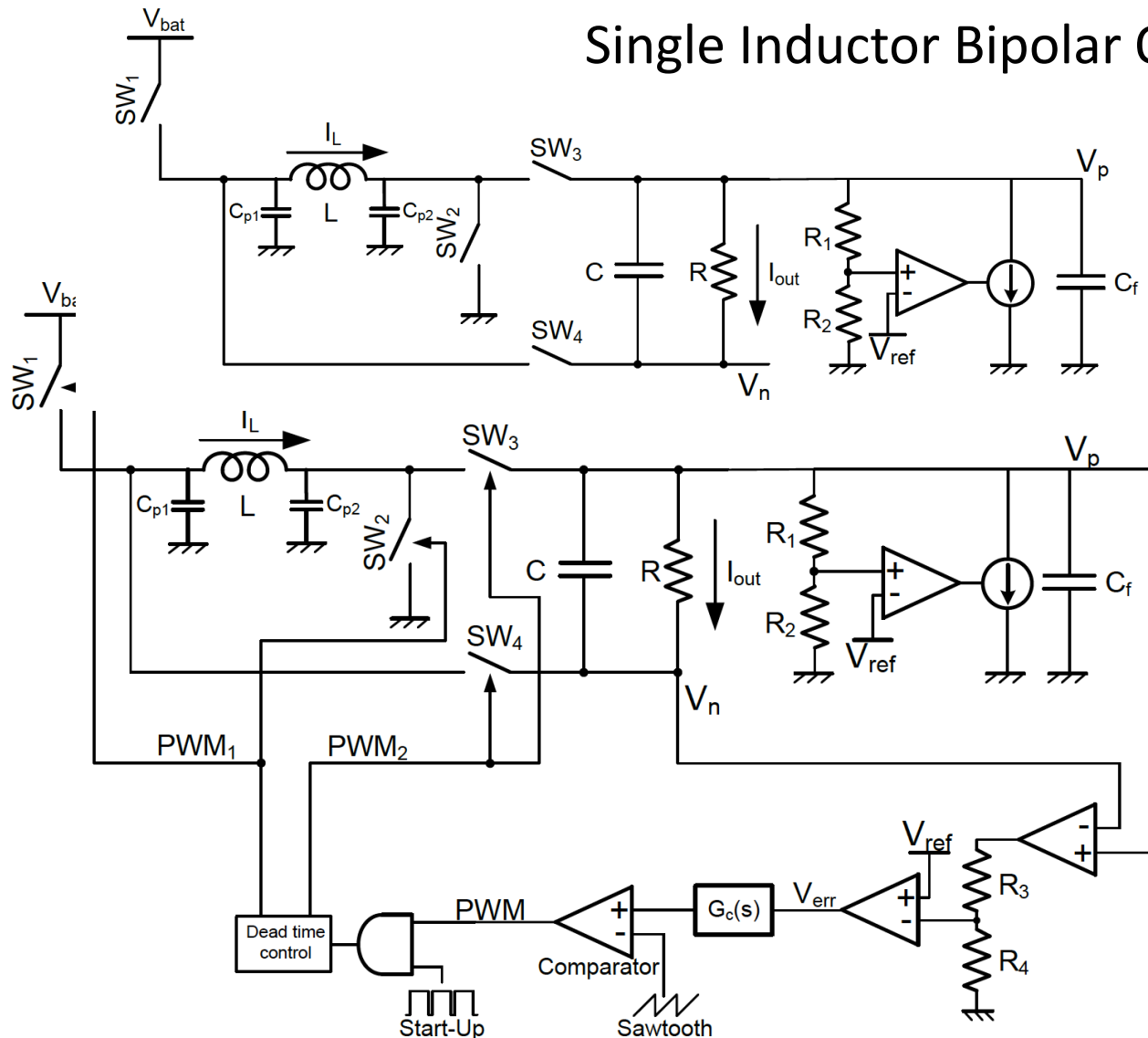
BASIC IDEA

Generate directly the difference between positive and negative voltage

Control the voltage of the positive terminal

2.5 SIBO DC-DC Converter

Single Inductor Bipolar Output



There are pulses of current caused by the charging and discharging of parasitic capacitors (SC equivalent resistances).

The currents reach the positive node

The current generator controlled by the op-amp compensates for the pulses of current and controls the positive output voltage

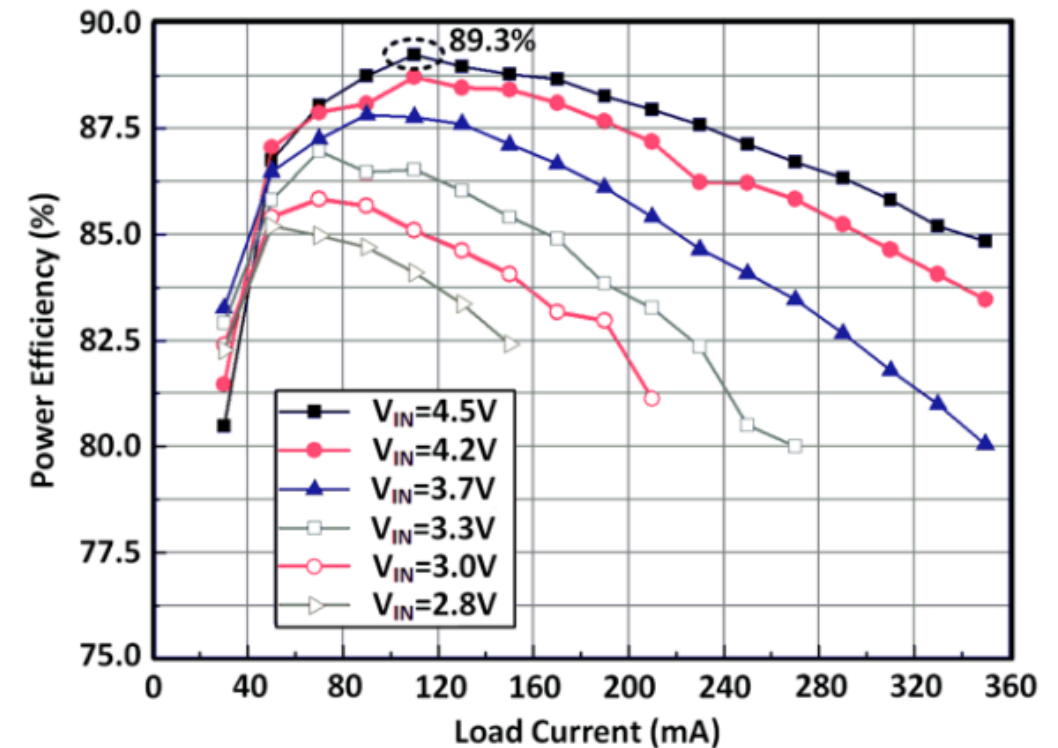
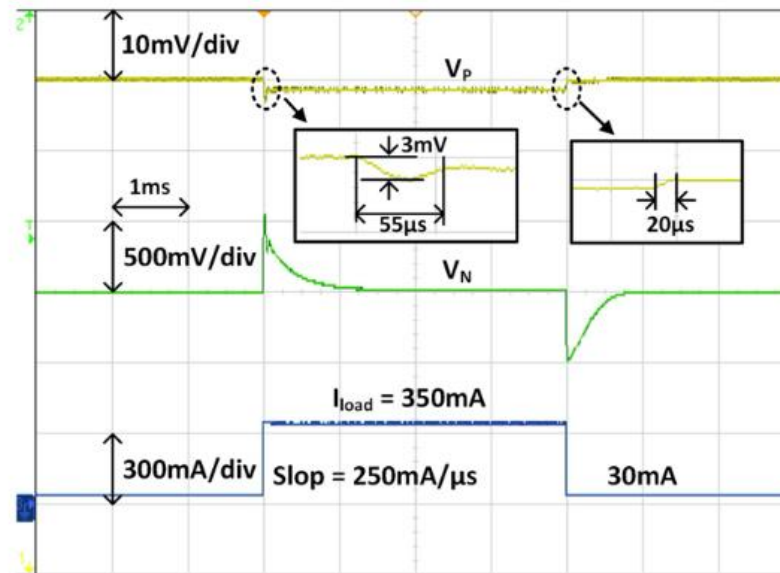
A second loop controls the differential output voltage.

2.5 SIBO DC-DC Converter

Single Inductor Bipolar Output

A modified version has been integrated by a PhD student in Macau. (paper at CICC 2020)

	This Work	
Process	0.35 μ m 5V devices	
Chip Area (mm ²)	3.68	
Frequency (MHz)	1	
Inductor (μ H)	10	
Flying Cap (μ F)	4.7	
Max Eff.	89.3 % @1.1W	
Input Range	2.7~4.5V	
Max Power (W) @ $V_{IN} = 3.7V$ & Eff.> 80%	3.5	
Output Voltage (V)	V_P	V_N
	5.3	-4.7
Output Cap (μ F)	10+1	
Line Regulation (mV/V)	18	2
Load Regulation (mV/mA)	0.1	0.06
Output Ripple(mV)	@ 30~350mA	
	≤ 1	≤ 30

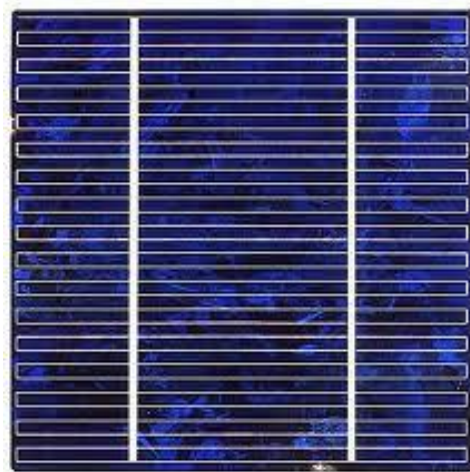
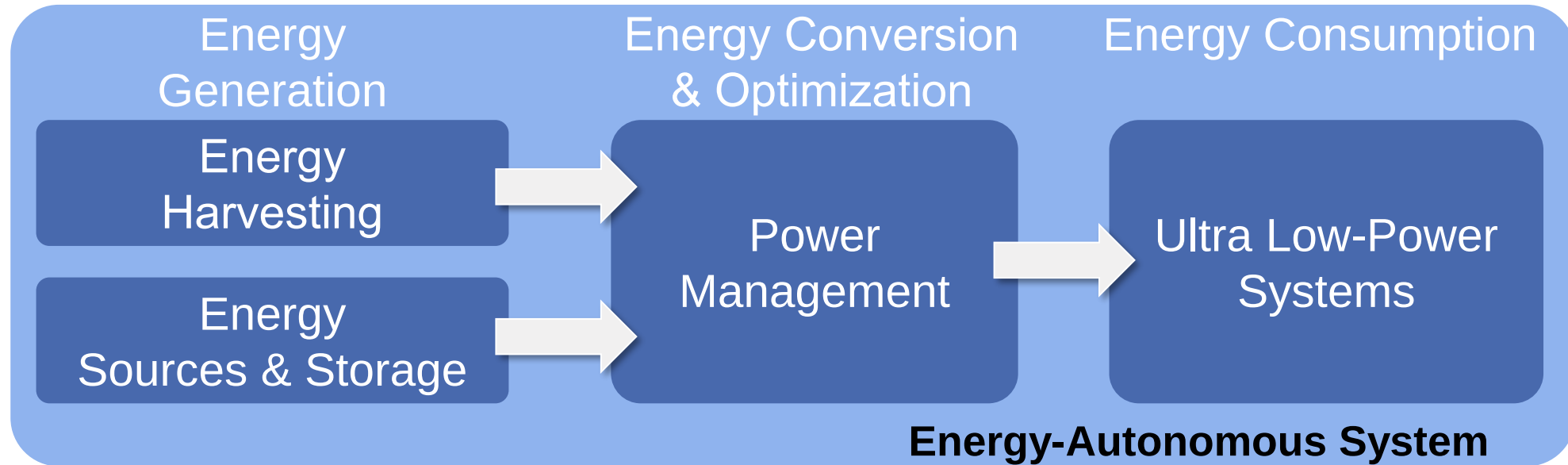


3. Energy Storing and Management

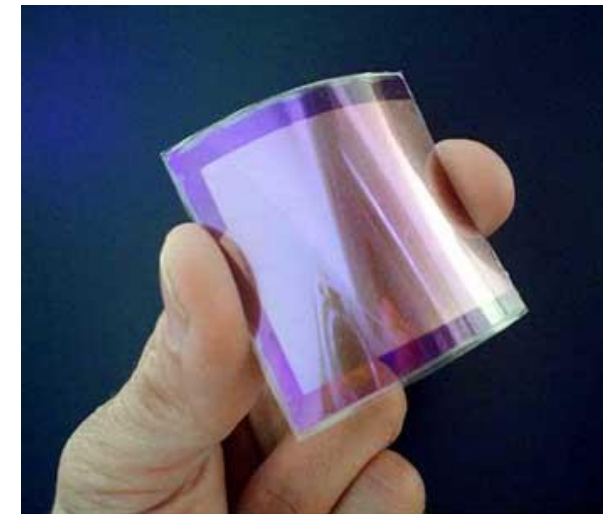
Content

- 3.1 Energy Harvesting and Storing
- 3.2 Maximum Power Point Tracking Circuits
- 3.3 Conversion circuits for AC transducers
- 3.4 Battery charging

3.1 Energy Harvesting and Storing



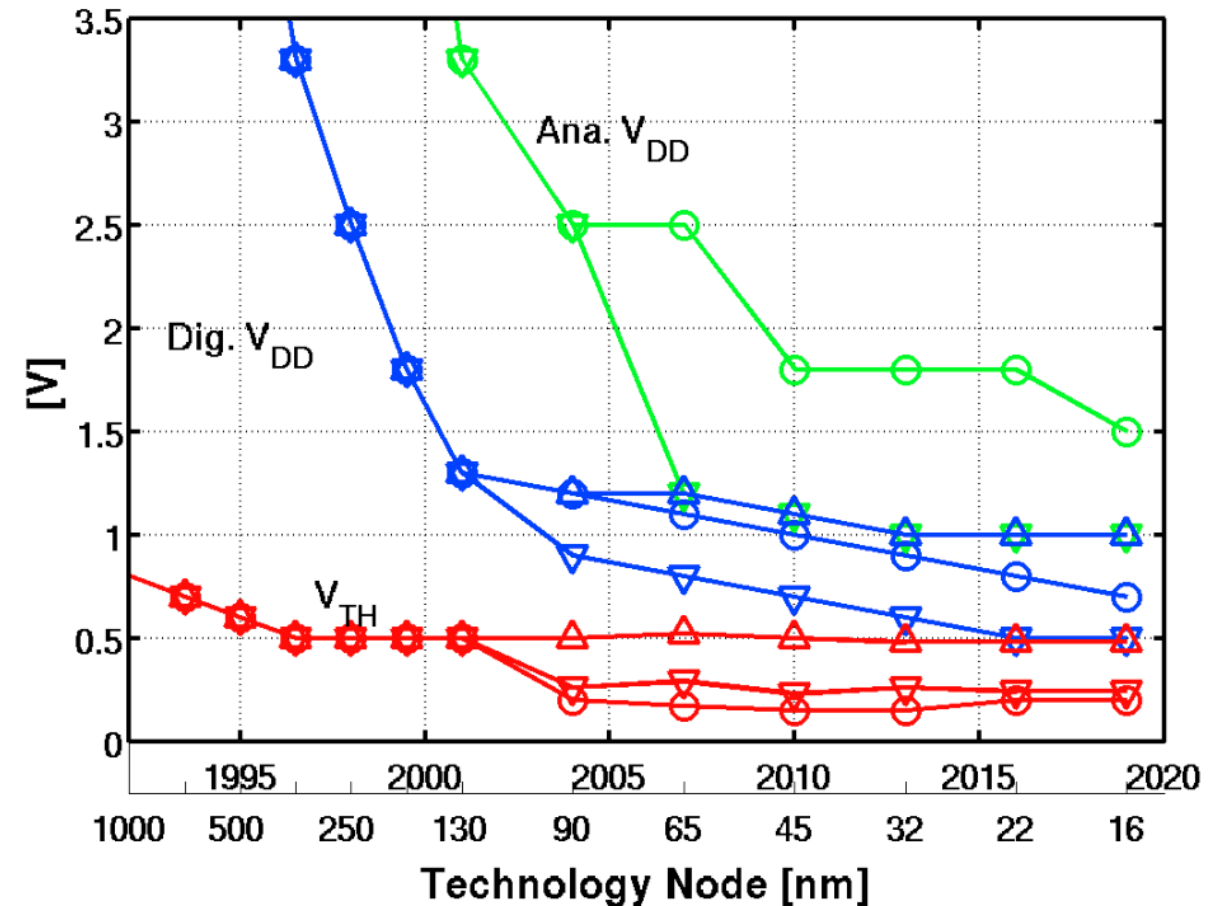
Efficiency 14.6%----Pmax 1.46W



3.1 Energy Harvesting and Storing

Supply Voltage Trend

- Depends on the technology node
- In mixed A/D circuits it is recommended using the same supply voltage in analog and digital sections
- For analog circuits don't use ultra-low transistor sizes (and related technologies)
- For ultra-low power do use ultra-low transistor sizes (for minimum capacitance to be charged and discharged).



3.1 Energy Harvesting and Storing

Low V_{DD} good for reducing the power consumption but challenging for designer

Use of special design techniques (like the use of the substrate terminal for signal)

Use of data converter architectures not demanding performant blocks

Use data converters architectures that don't use op-amps

Use of architectures with minimum voltage swings

Use, if useful for reducing power, digital assisted analog

3.1 Energy Harvesting and Storing

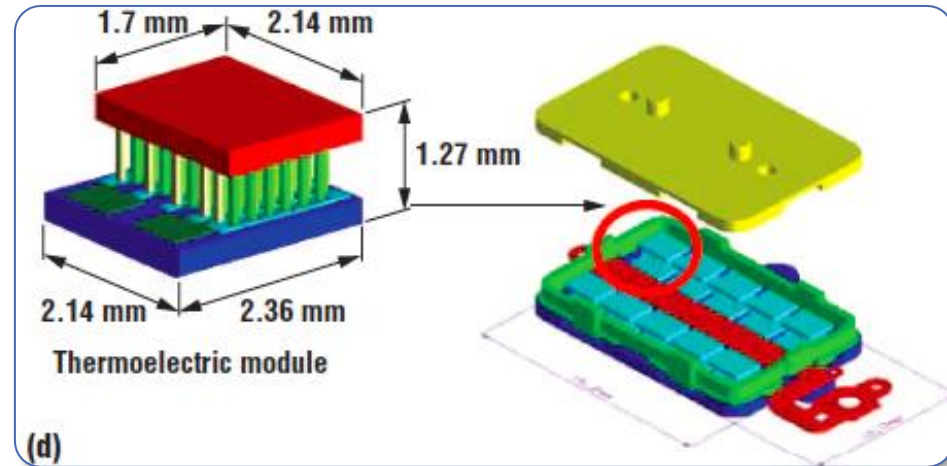
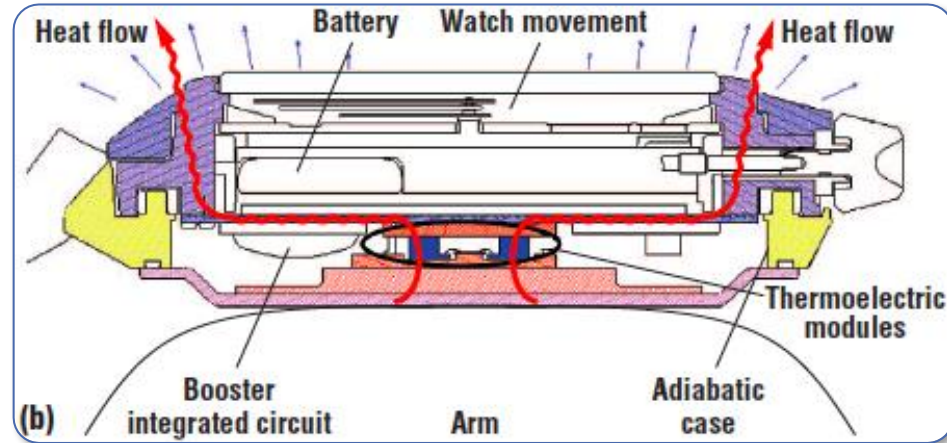
- Different sources,
But very-low power
- Light
- Thermal
- Vibration
- RF
- Wind
- Biosensor

POWER DENSITY OF ENERGY HARVESTING TECHNIQUES.

Energy harvesting technique	Power density
Photovoltaic	Outdoors (direct sun): 15 mW/cm ² Outdoors (cloudy day): 0.15 mW/cm ² Indoors: <10 μ W/cm ²
Thermoelectric	Human: 30 μ W/cm ² Industrial: 1 to 10 mW/cm ²
Piezoelectric	250 μ W/cm ³ 330 μ W/cm ³ (shoe inserts)
Electrostatic	50 to 100 μ W/cm ³
Electromagnetic	Human motion: 1 to 4 μ W/cm ³ Industrial: 306 μ W/cm ³
RF	GSM 900/1800 MHz: 0.1 μ W/cm ² Wifi 2.4 GHz: 0.01 μ W/cm ²
Wind	380 μ W/cm ³ at the speed of 5 m/s

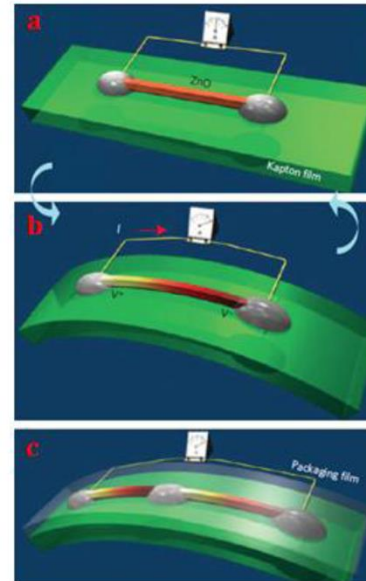
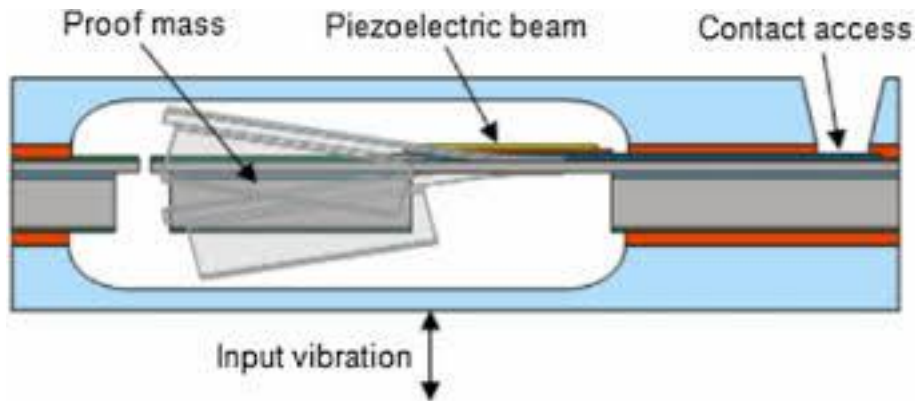
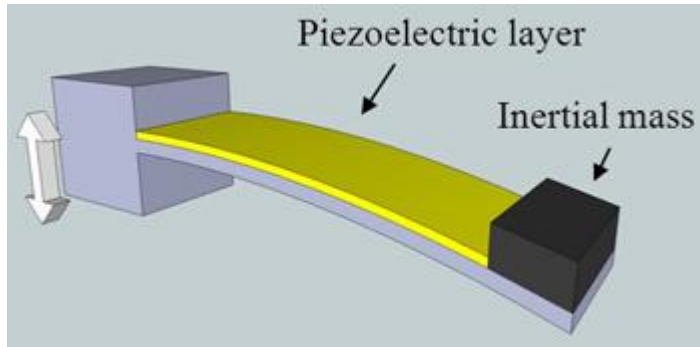
3.1 Energy Harvesting and Storing

Thermoelectric

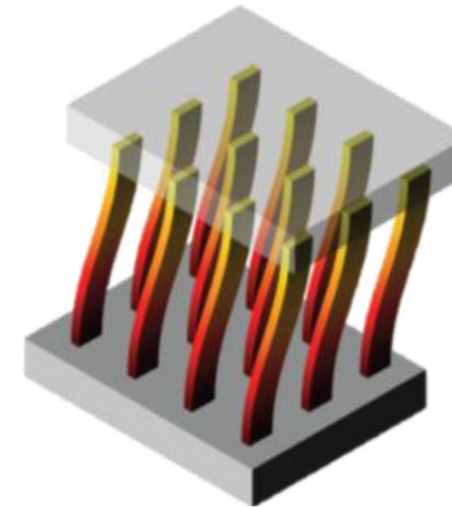


3.1 Energy Harvesting and Storing

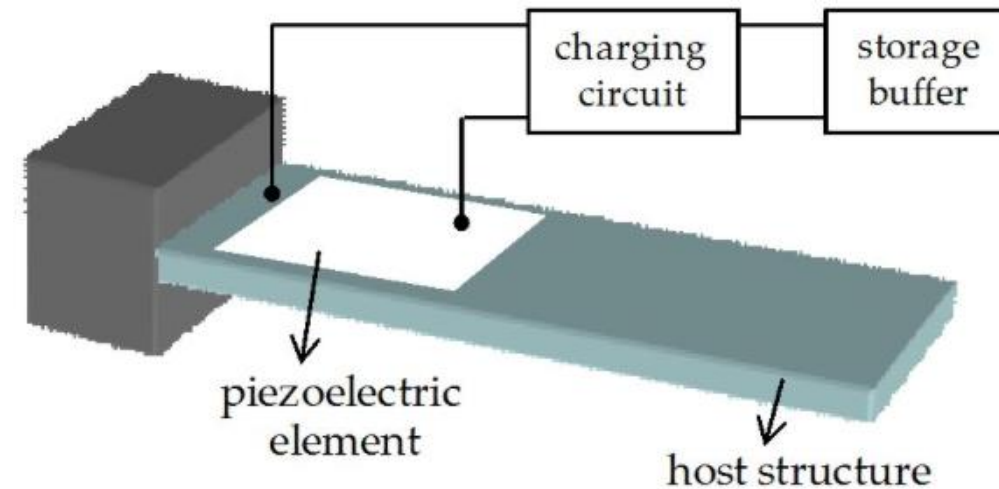
Mechanical energy: Piezo-devices



on flexible substrate



Nano ribbon

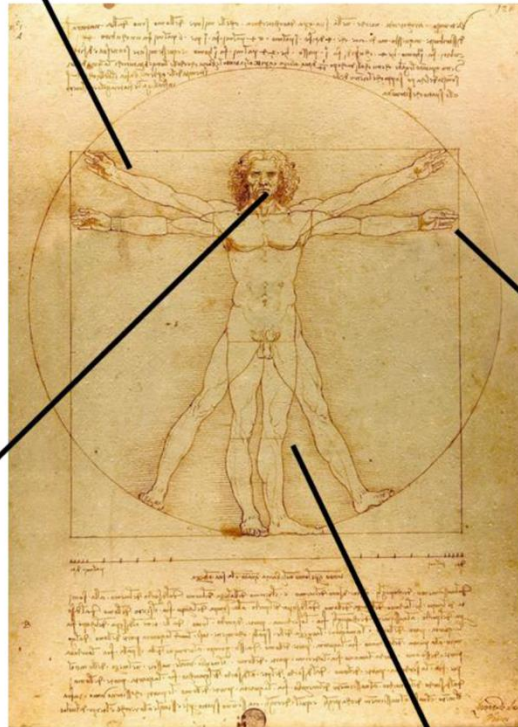


Piezoelectric Energy Harvesting Solutions
Sensors **2014**, 14(3), 4755-4790;

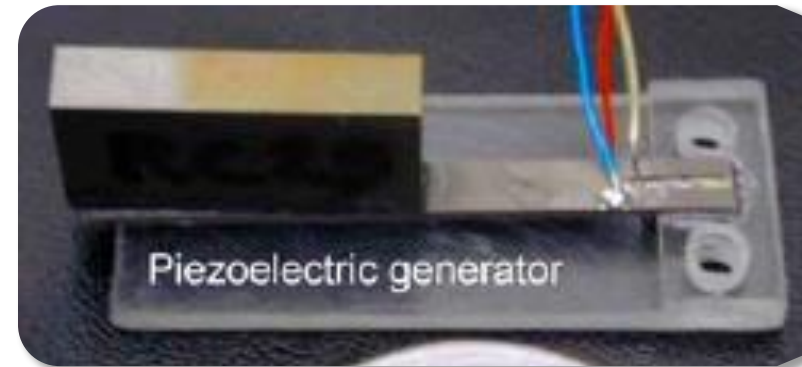
3.1 Energy Harvesting and Storing

Mechanical energy from human body

Upper limbs: ~10 mW



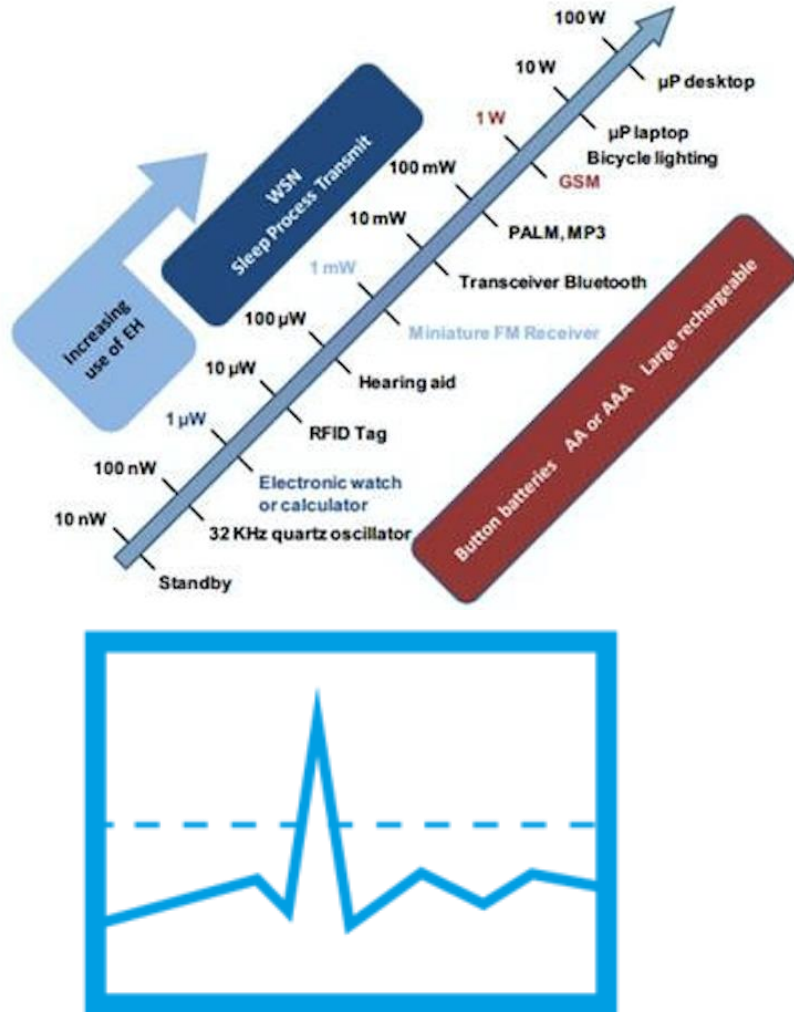
Typing: ~1 mW



Walking: ~1 W

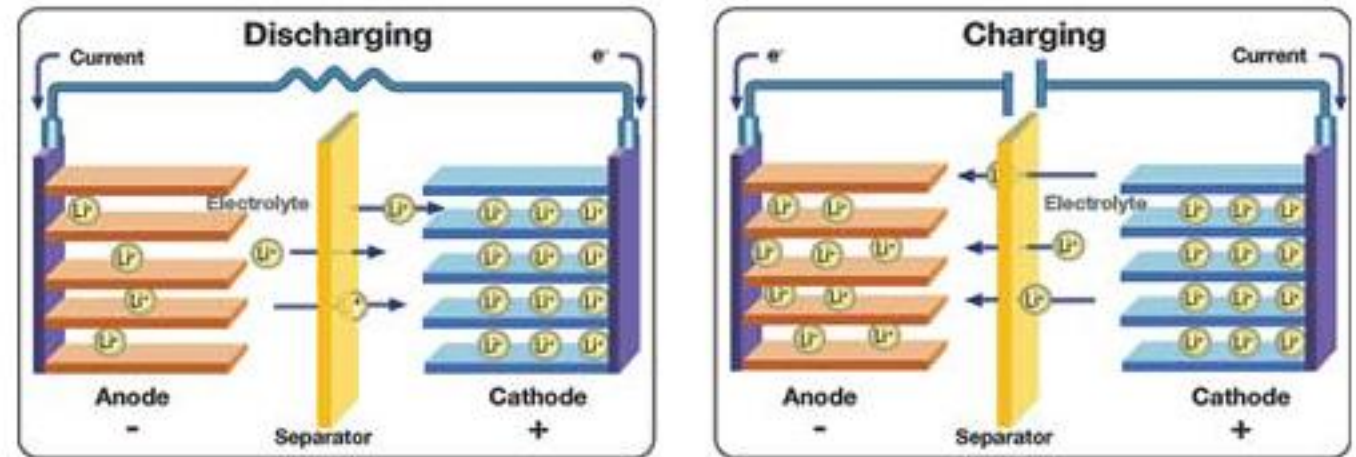
3.1 Energy Harvesting and Storing

Why we need to Store Energy



How can we Store Energy

Gasoline: specific energy, ~ 46.4 MJ/kg
Li-metal: specific energy, ~ 1.8 MJ/kg
Li-ion: specific energy, ~ 0.9 - 2.6 MJ/kg
Alkaline: specific energy, ~ 0.5 MJ/kg
Lead-acid: specific energy, ~ 0.17 MJ/kg
SuperCap: specific energy, ~ 0.101 MJ/kg



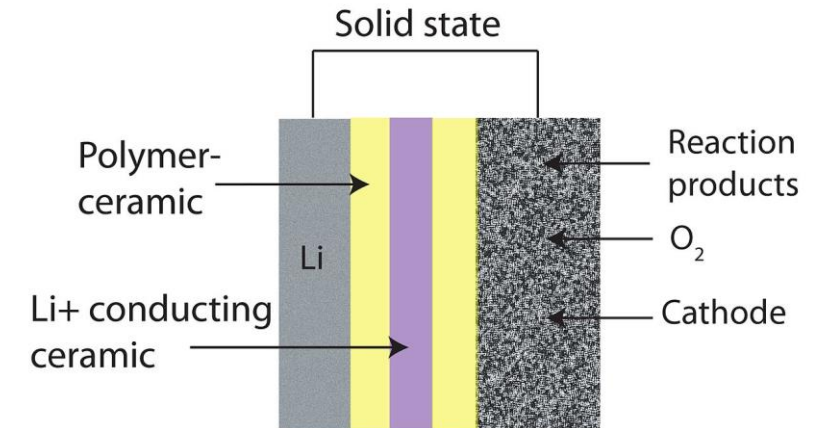
LI-ion Battery

3.1 Energy Harvesting and Storing

- **Lithium ion polymer battery** (LIPB, secondary, rechargeable)
 - Anode: Li metal, Li-carbon
 - Cathode: LiCoO_2 , LiMn_2O_4 , LiFePO_4
 - Electrolyte: Li^+ conducting polymer (PVdF, PEO) w/ Li salt
 - OCV: 3.6-3.7 V
 - Energy density (mass): 250 Wh/Kg $\sim 0.9 \text{ MJ/Kg}$

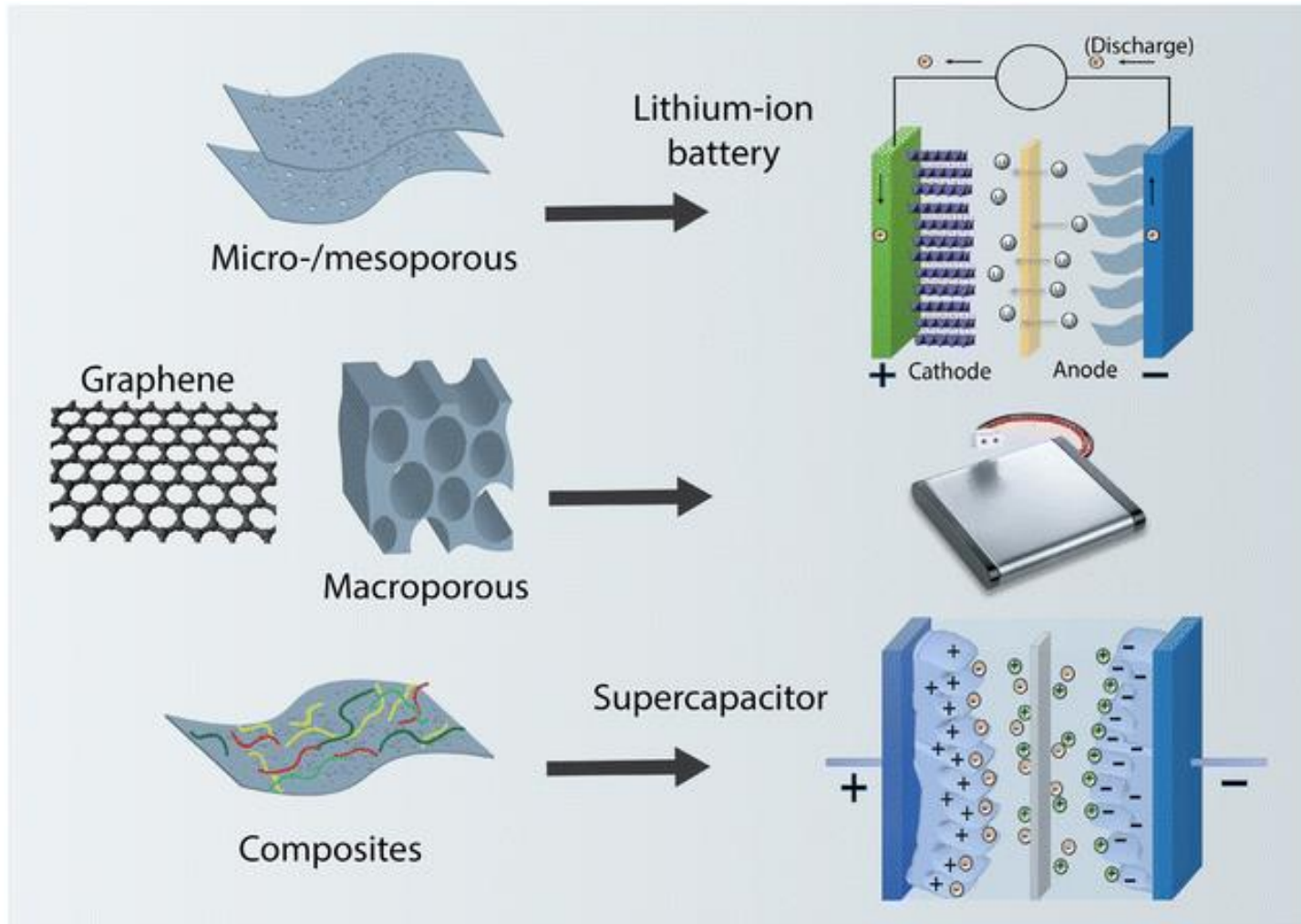


- **Lithium air battery** (LAB, primary or secondary)
 - Anode: Li metal
 - Cathode: graphite (w/catalyst)
 - Electrolyte: LiPF_6 in organic carbonates, PVdF
 - OCV: 2.9 V
 - Energy density (mass): 5000 Wh/Kg $\sim 18 \text{ MJ/Kg}$

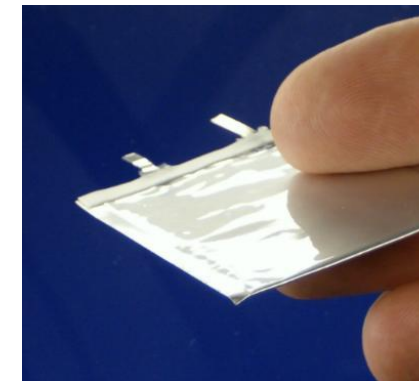
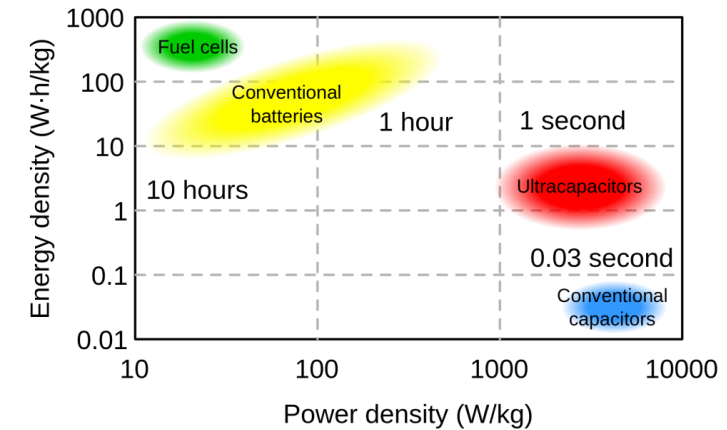


Solid state-like Li-Air battery

3.1 Energy Harvesting and Storing



Porous Graphene for Energy Storing

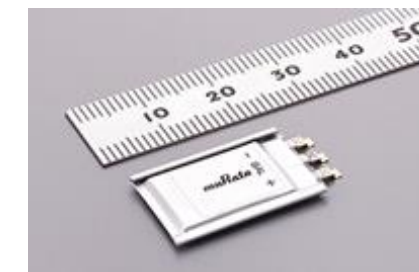


POWERSTREAM

2 mAh/cm²

3.6V (25.9 J)

12 x 12 x 2 mm



MURATA

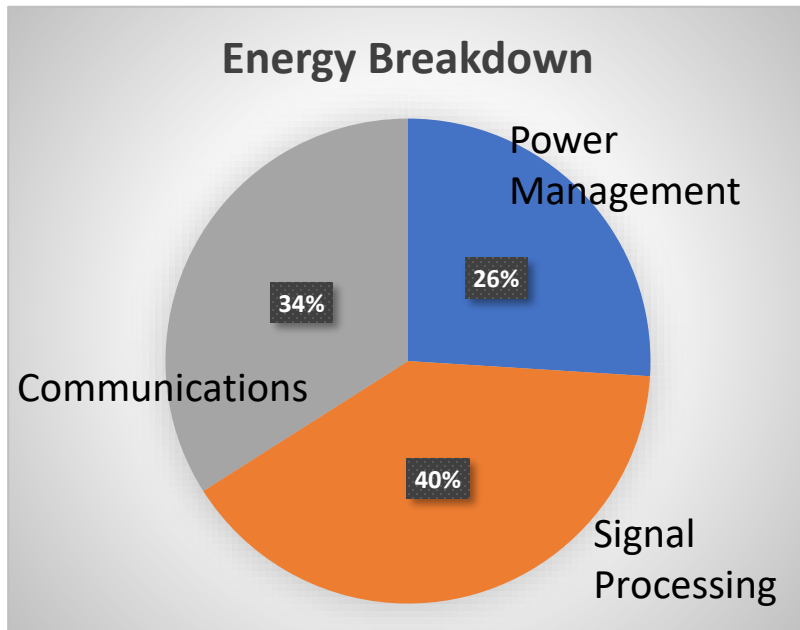
4.2 V 470 mF

(8.3 J)

25 x 14 x 3.5 mm

3.1 Energy Harvesting and Storing

- The power harvested is in the tens of μW range
- The energy stored can be about 10-20 J
- The key issue is on how to budget energy/power



Communic POWER

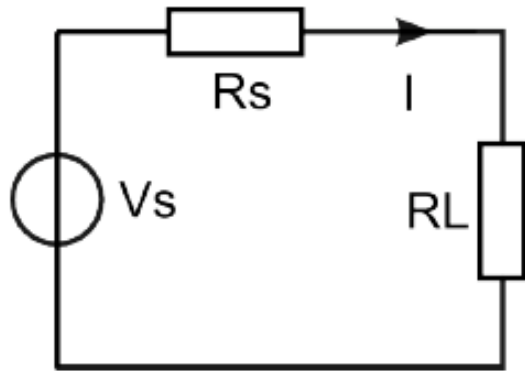
- Transmit
- Receive
- Duty cycle
- Data-rate

Sign Proc POWER

- Sensor(s)
- Analog interface
- Data Conversion
- DSP

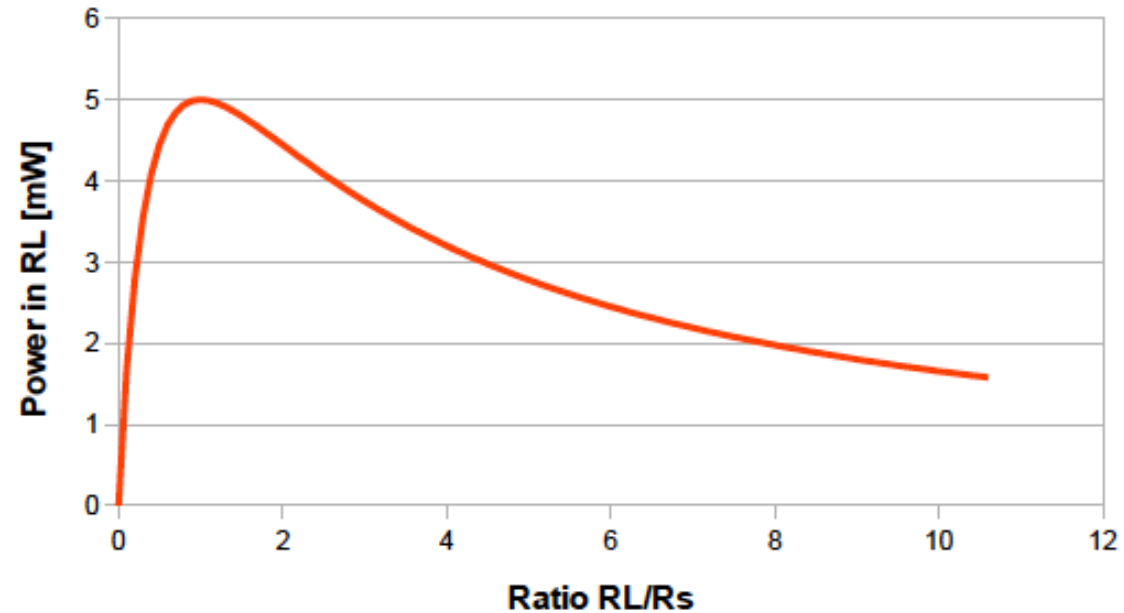
3.2 Maximum Power Point Tracking circuits

Source and load impedance matching



$$P_L = V_s^2 \cdot \frac{R_L}{(R_L + R_s)^2}$$

Example with $V_s = 1\text{ V}$, $R_s = 50\text{ Ohm}$



Power P_L transmitted to the load is optimized when $R_L = R_s$

Voltage converters must provide impedance adaptation for optimal power transfer

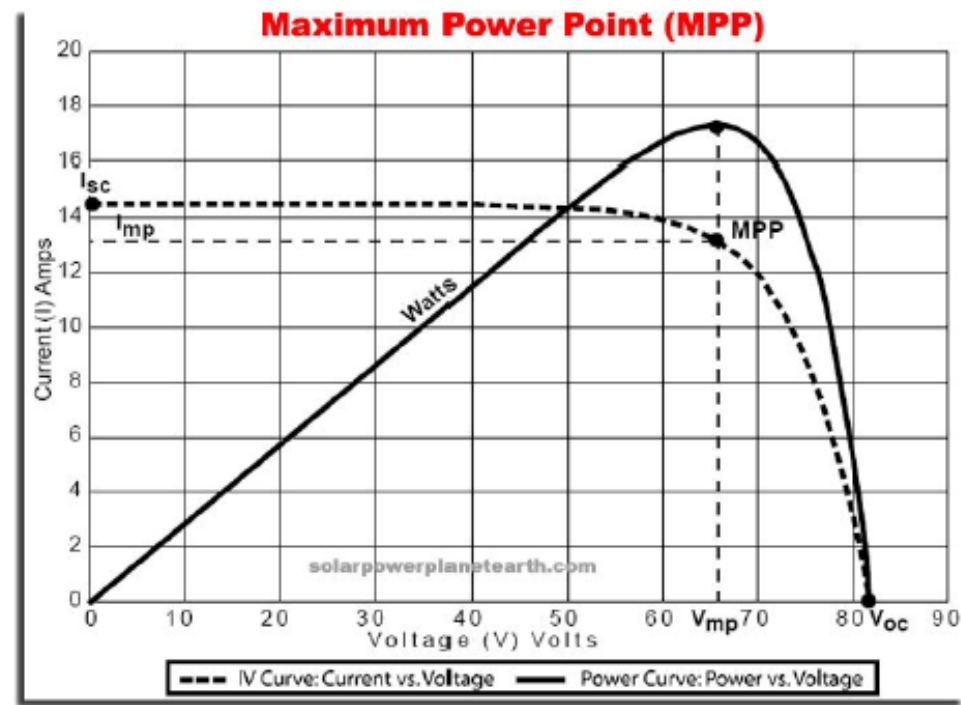
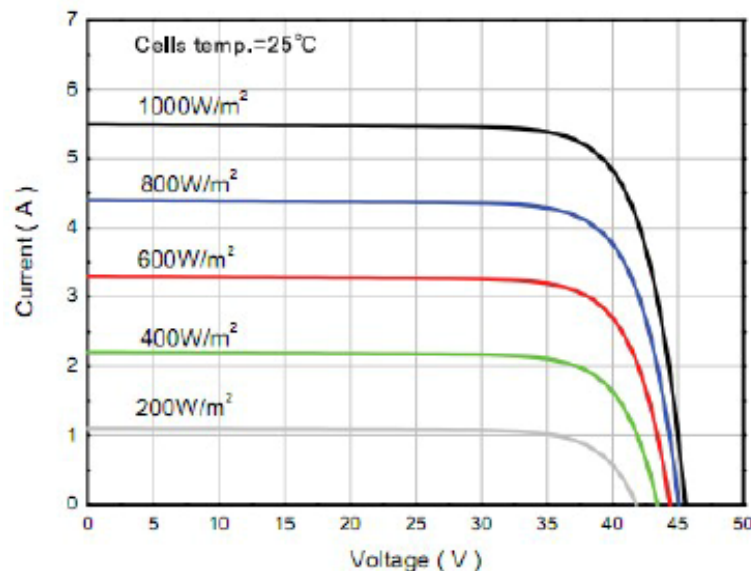
If $R_L \gg R_s$, (rare in energy scavenging!!), impedance matching is not required

3.2 Maximum Power Point Tracking circuits

Typical solar cell I-V response curve

The extracted power from a solar cell depends strongly on the operating point :

- if too much current is extracted (too small load resistance), the voltage drops and the power drops as well
- if too small current is extracted, the power is not fully exploited.



3.2 Maximum Power Point Tracking circuits

Maximum Power Point Tracking (MPPT)

Definition

The process of finding and tracking the operating point with maximum power
Can be applied to any I-V characteristics, whether purely resistive, or complex (inductive – capacitive) or from a semiconductor device (solar panels).

Methods

Perturb and observe
Incremental conductance
Current sweep

3.2 Maximum Power Point Tracking circuits

Perturb and observe method

Principle

Starting from the actual load resistance value, the algorithm performs iteratively :

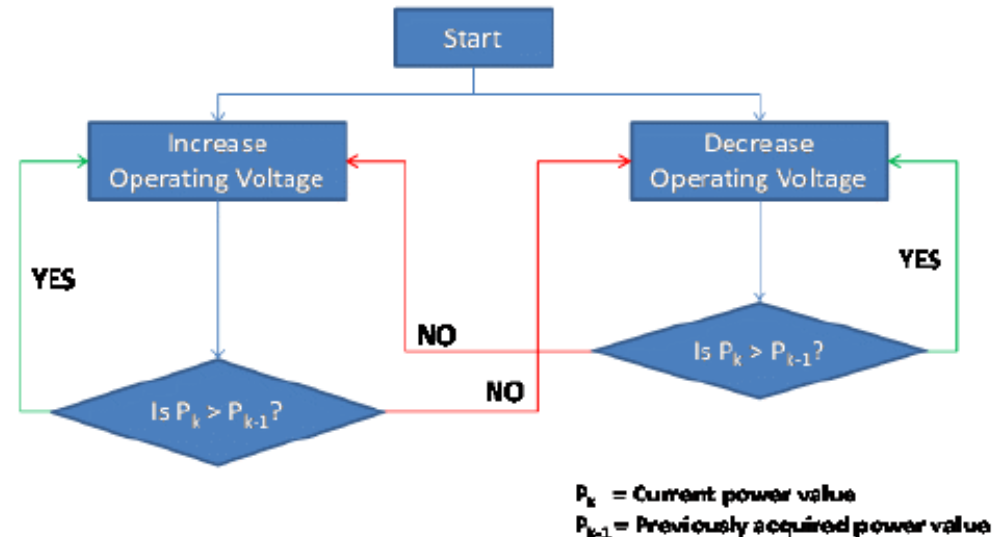
- It adjusts the controller load resistance value, and measures the power
- If the power increases, this new load resistance value is adopted. A new adjustment in the same direction is done
- If it decreases, the algorithm adjusts the load resistance in the opposite direction

Advantages

- Ease of implementation, highest power obtained.

Drawbacks

- May produce power oscillations around the maximal point.



3.2 Maximum Power Point Tracking circuits

Incremental conductance method

Principle

At MPP, the conductance I/V equals the negative instantaneous conductance dI/dV . Proof : $DP/dV = 0 \rightarrow d(I/V)/dV = I/V + V(dI/dV) \rightarrow I/V = - dI/dV$

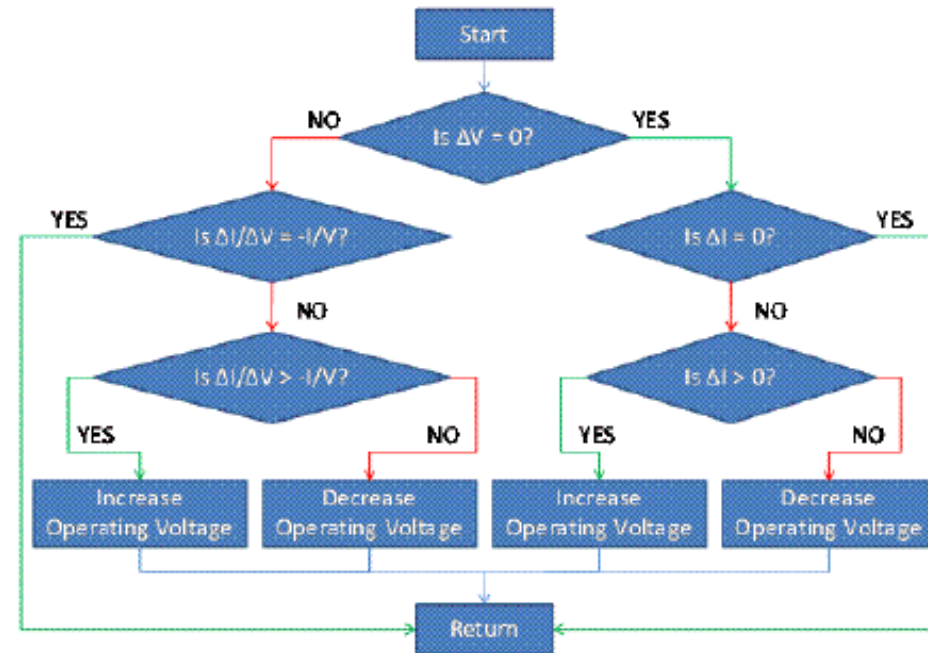
The incremental conductance method observes any change in I or V and deduces a correct adjustment of operating voltage to stay at the MPP.

Advantages

- No oscillation around MPP.
- Rapid convergence to MPP.

Drawbacks

- Higher complexity
- Can behave erratically under Rapid changing conditions.



3.2 Maximum Power Point Tracking circuits

Current sweep method

Principle

The current of the source is swept to obtain the IV characteristics of the transducer. The MPP voltage is then computed.

Advantages

- Absolute maximal always found.

Drawbacks

- Complete stop of energy extraction during the sweep.

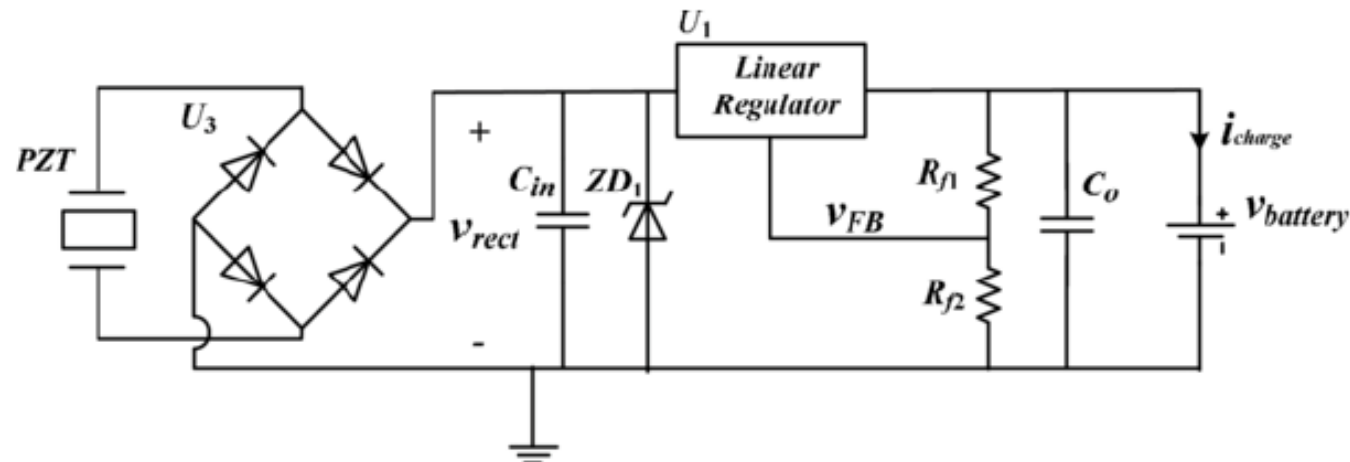
3.3 Conversion circuits for AC transducers

AC transducers

Piezoelectric energy harvesters : provide an AC voltage with amplitude proportional to acceleration and proof mass. Typical parallel capacitance C_p is 20 nF and parallel resistance R_p is 500 kOhm.

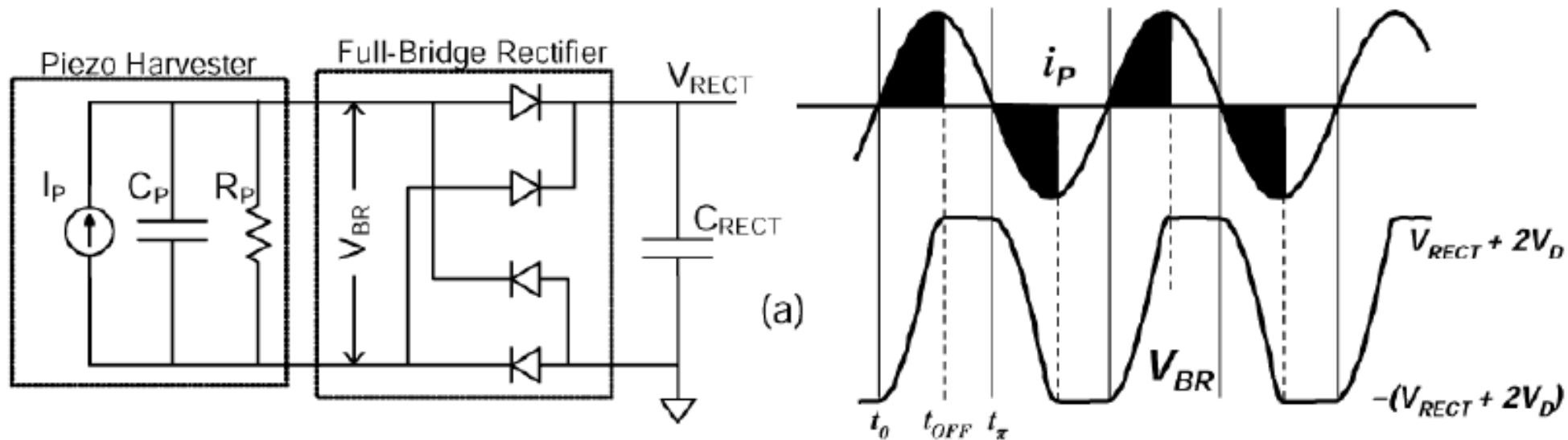
Other AC transducers (electromagnetic) provide also an AC voltage from which energy has to be extracted.

Typical signal conditioning circuit : diode rectifier, zener diode to limit the voltage, then regulator to provide the useful voltage.



3.3 Conversion circuits for AC transducers

Piezoelectric energy harvester with diode rectifier

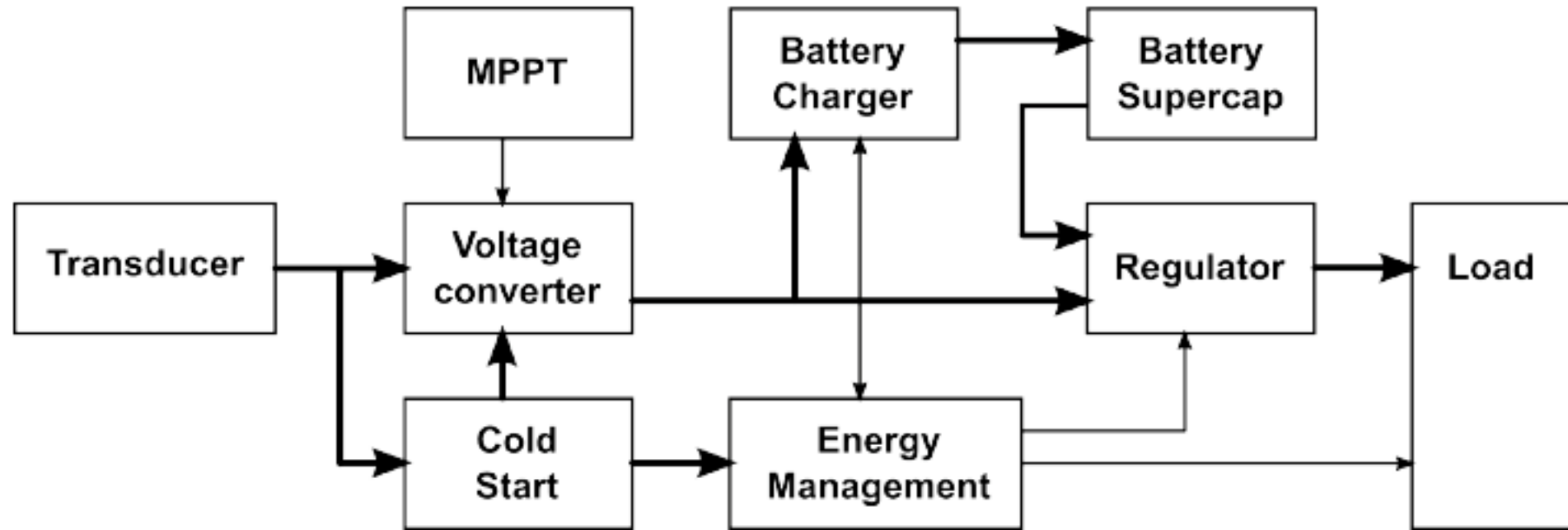


The shaded zones of the piezo current represent the current going into C_P (and not useful to load C_{RECT}) --> poor energy extraction !

Further losses are caused by the diode voltage (0.4 to 0.7 Volt) which may not be a problem for high voltage generators, but which represent a serious limitation in case of low vibration amplitude.

3.4 Battery Charging

Typical energy harvesting system with energy storage

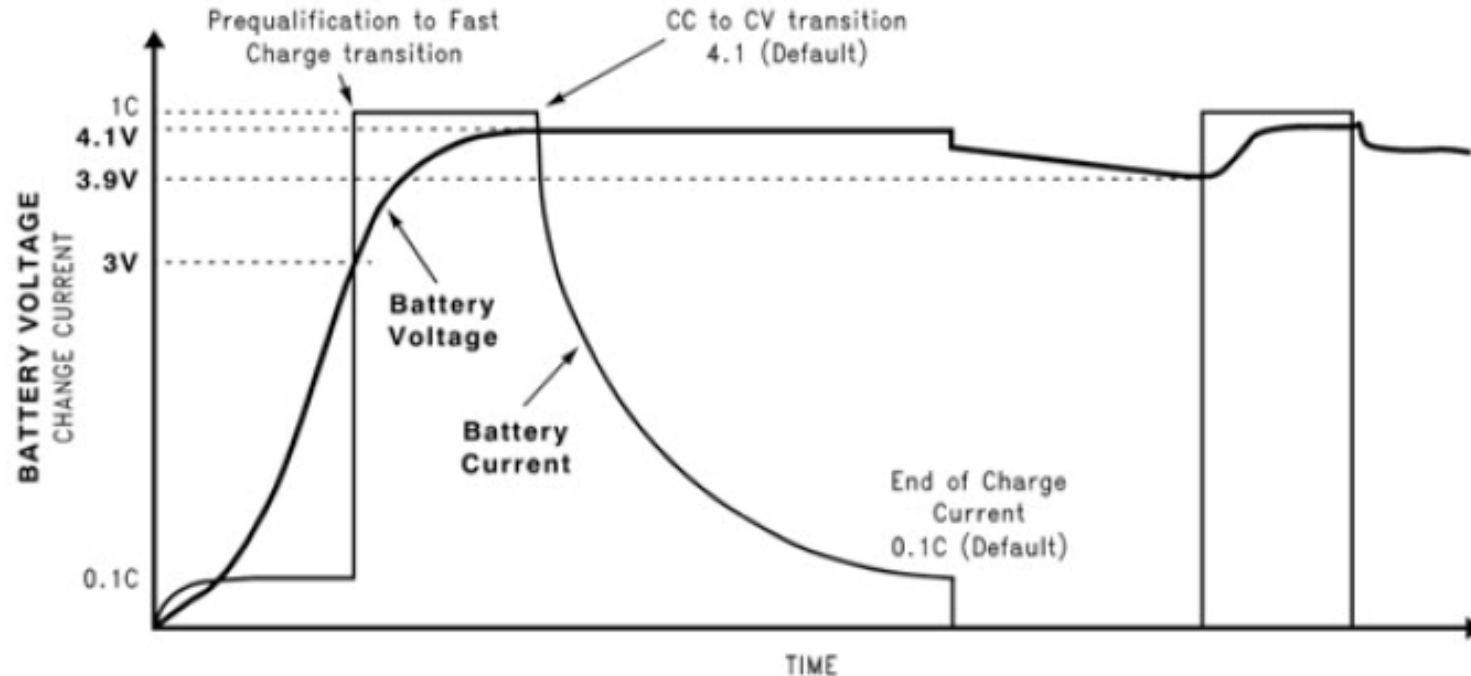


3.4 Battery Charging

Lithium batteries

Conversion : C = current equivalent to battery capacity divided by 1 hour

1. Pre-conditioning charge with $0.1C$ when the battery is deeply discharged
2. Constant current charge. The higher the current the lower the capacity
3. Constant voltage charge. The current gradually goes down
4. End of charge when the current goes below $0.1C$



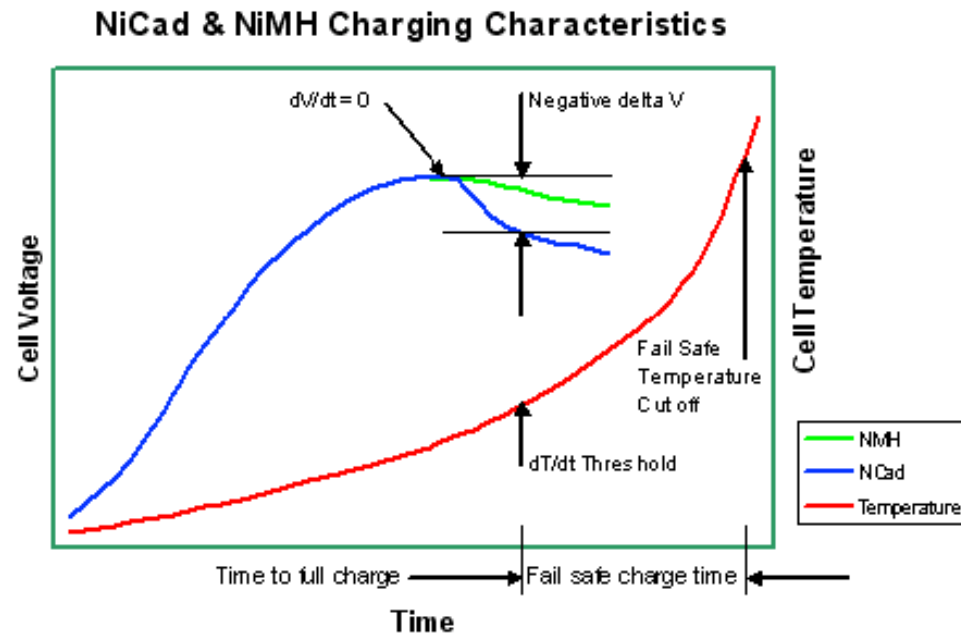
3.4 Battery Charging

Ni-MH batteries

These batteries can be damaged or even dangerous when overcharged.

1. Constant current charge. The cell temperature increases
2. End of charge : 1/ detect negative dV/dt , 2/ timer, 3/ Temperature
3. After charge : trickle charging with C/300 or low duty cycle charge at C/10

The charge temperature is very important.



3.4 Battery Charging

General description

Needed building blocks

- Measurement of charge and discharge current
- Measurement of battery voltage (absolute accuracy important!)
- For safety : measurement of battery cell temperature
- Constant current or constant voltage sources
- Battery chemistry detector (generally configuration bits)
- Switch to disconnect the battery in case of deep discharge / short circuit
- State machine to perform battery charge profile and monitoring

Charging functionality

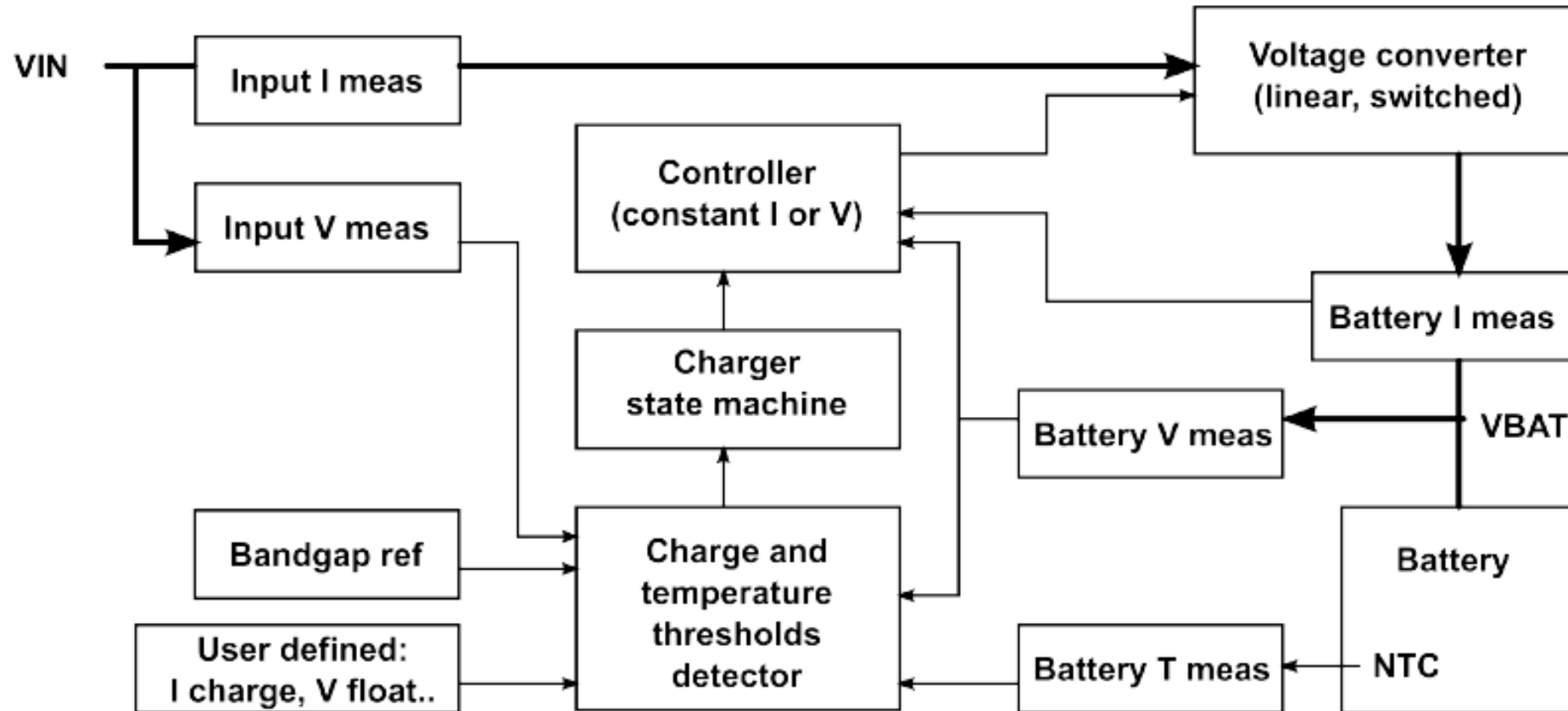
- Measure the battery voltage and determine the charge state
- Apply the charge profile, monitor the voltage/current

Monitoring / safety functionality

- Measure temperature and stop charge/discharge when abnormal
- Measure discharge current and disconnect the battery when abnormal
- Periodically measure battery capacity check

3.4 Battery Charging

Typical battery charge/management circuit diagram

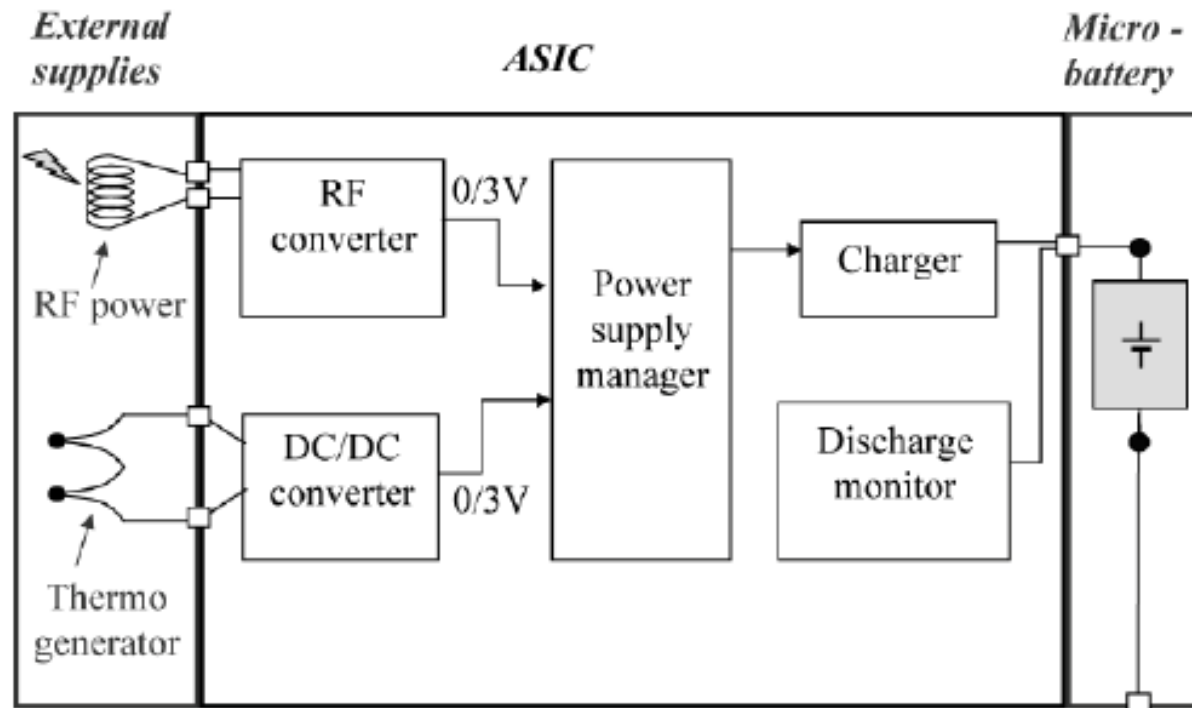


3.4 Battery Charging

Academic example : thin-film Lithium battery charger

Efficient Power Management Circuit: From Thermal Energy Harvesting to Above-IC Microbattery Energy Storage, H. Lhermet, IEEE JSSC, Vol 43, No 1, Jan 2008.

The battery charger and manager is part of a complete harvesting system with RF power receiver, thermogenerator and above-IC deposited microbattery

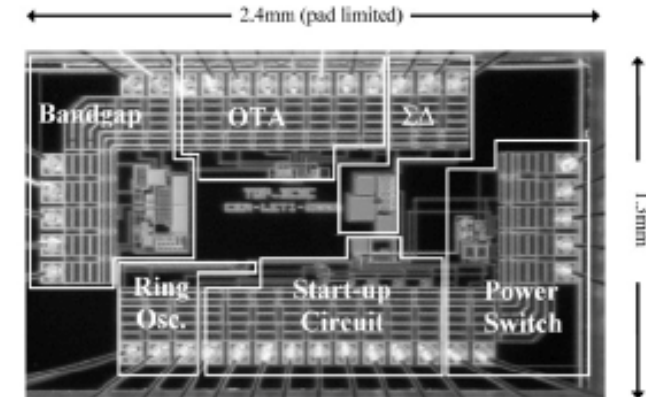
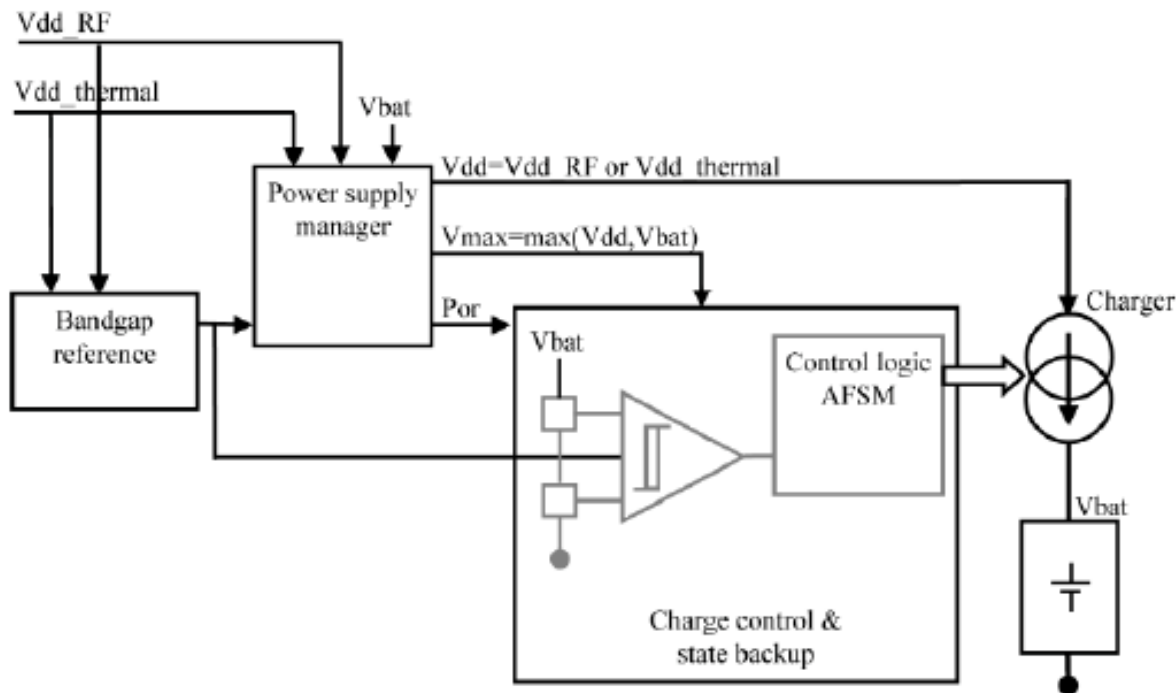


3.4 Battery Charging

Academic example : thin-film Lithium battery charger (II)

Microbattery state of charge monitor : lowest power for long battery operation.

- power supply manager taking the highest supply (RF or thermal) for charge
- the manager switches to battery power in case of external voltage failure
- constant-current battery charge (27 μA) with over charge monitoring
- state of charge monitor with detection of undercharge : 5 nW of Pcons



3.4 Battery Charging

Commercial example : Linear LTC4071 LiPO shunt battery charger

Simple charger in constant current mode. The current is fixed by V_{in} , R_{in} and the battery voltage : $I_{chg} = (V_{in} - V_{bat}) / R_{in}$. When the float voltage is reached, the charge current is shunt to GND through MP2. Specially suited for energy harvesting.

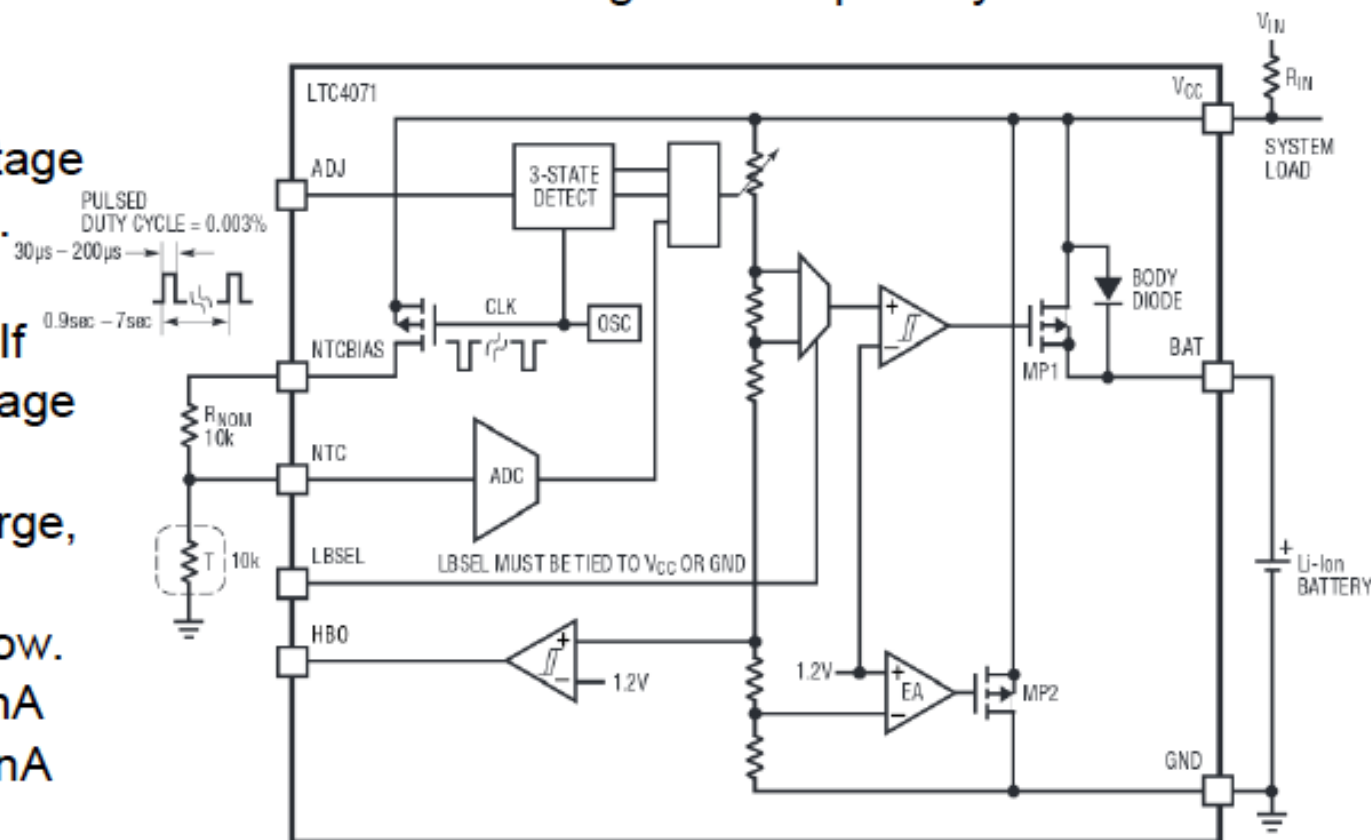
4.0/4.1/4.2 V float voltage
selected with pin ADJ.

Battery temperature sensed with an NTC. If too high, the float voltage is reduced.

To avoid deep discharge, MP1 disconnects the battery when vbat is low.

Quiescent curr : 550 nA

Disconnect curr : 0.1 nA



4. Sensor Electronics

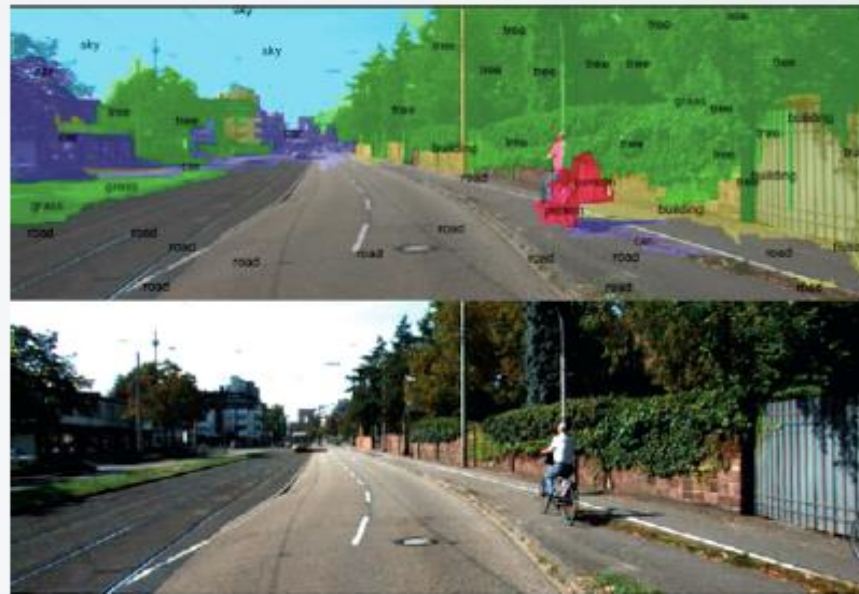
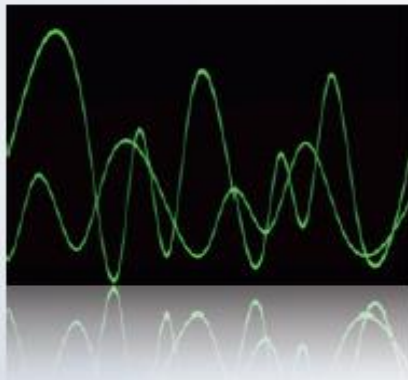
Content

- 4.1 Introduction
- 4.2 Magnetic sensors
- 4.3 Offset compensation

4.1 Sensor Electronics

SENSOR

- Sensors provide environmental information from the physical world.
- The **amount of information** we can extract from the real world via a sensor depends on how well the interface has been designed.



4.1 Sensor Electronics

Definitions

Microsensors and integrated microsystems

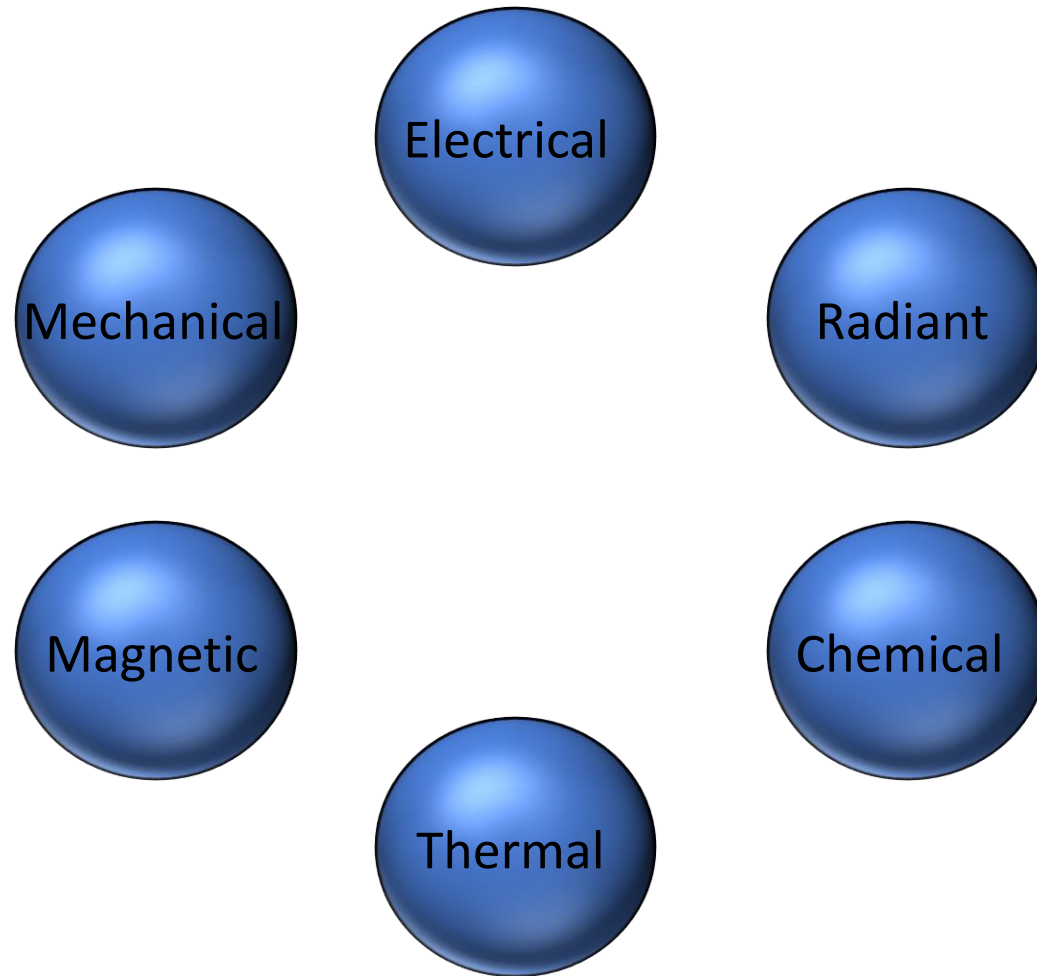
- **Microsensor** → Sensor realized with integrated circuit (IC) technologies
- **Microactuator** → Actuator realized with integrated circuit (IC) technologies
- **Integrated microsystem** → Complete system realized in miniaturized form using integrated circuit (IC) technologies
- **MEMS** → Micro-electro-mechanical system

Sensor classification

- **Active sensor** → Sensor that produces an **active electrical quantity** (voltage, charge, current) through energy conversion
- **Passive sensor** → Sensor that produces a variation of a **passive electrical quantity** (resistance, capacitance, inductance)

4.1 Sensor Electronics

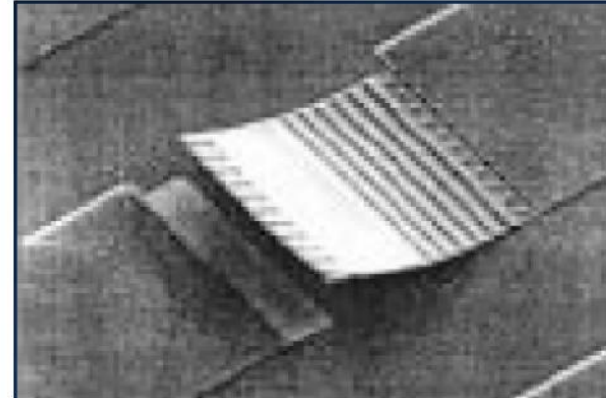
Sensors Signal Domains



4.1 Sensor Electronics

Mechanical

- MEMS switches
 - Used in RF applications
- Force
- Touch
- Acceleration
- Pressure
- Gyroscopes



4.1 Sensor Electronics

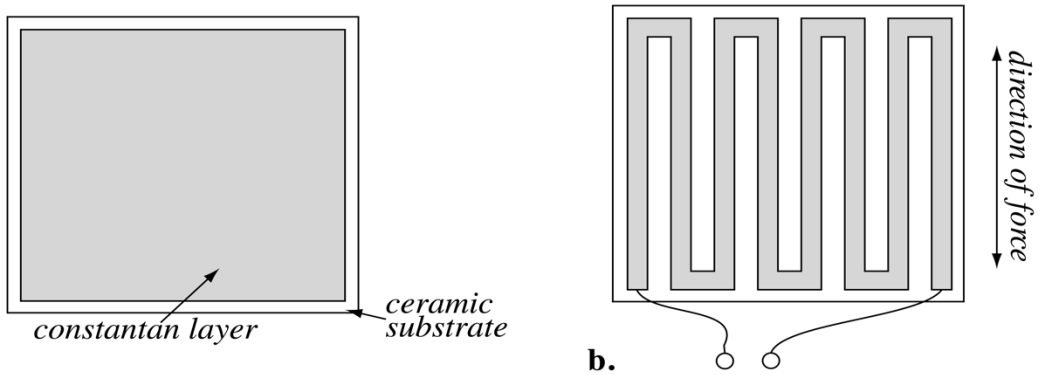
Force Sensor – Strain Gauge

- It is a metallic wire L , of conductivity σ , and cross-section area A .
- For small deformations (linear deformation), the resistance is a linear functions of strain, ϵ

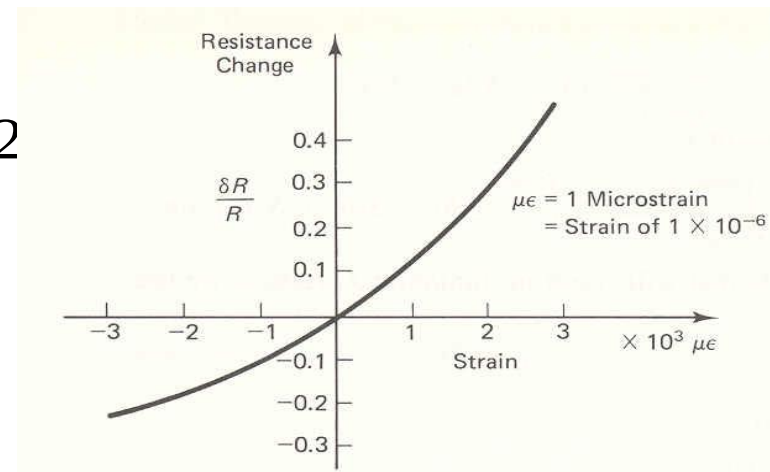
$$\frac{dR}{R} = - \frac{dS}{S} + \frac{d(L/A)}{L/A}$$

$$\frac{dR}{R} = S_s \epsilon$$

4.1 Sensor Electronics

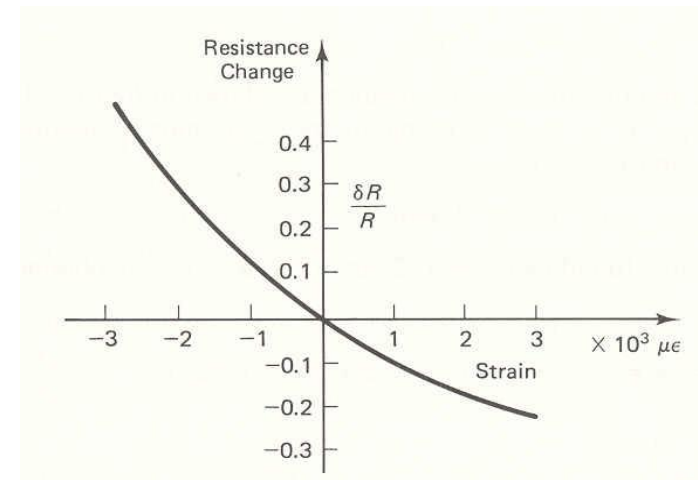


$$\frac{dR}{R} = S_1 \epsilon + S_2 \epsilon^2$$



Semiconductor strain gauges

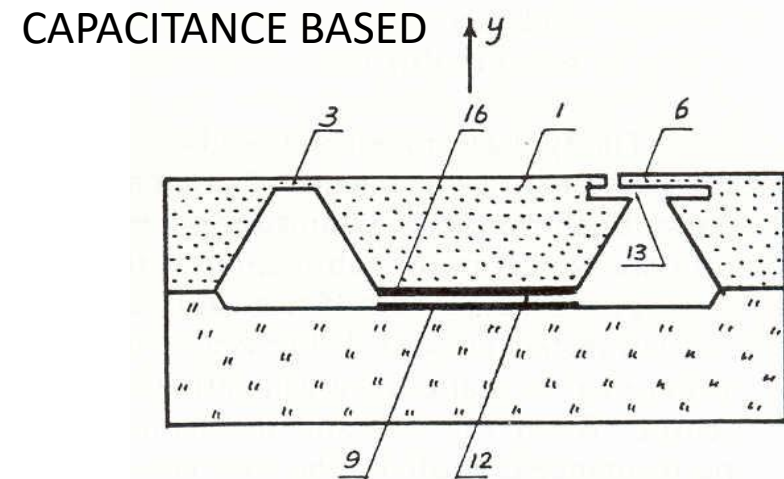
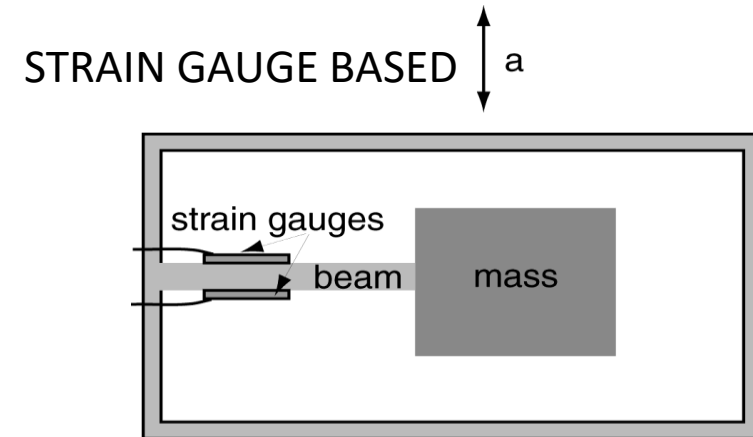
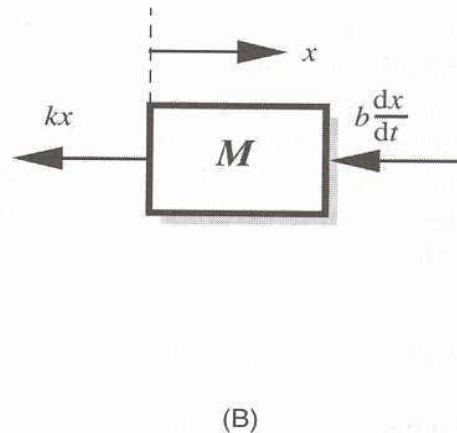
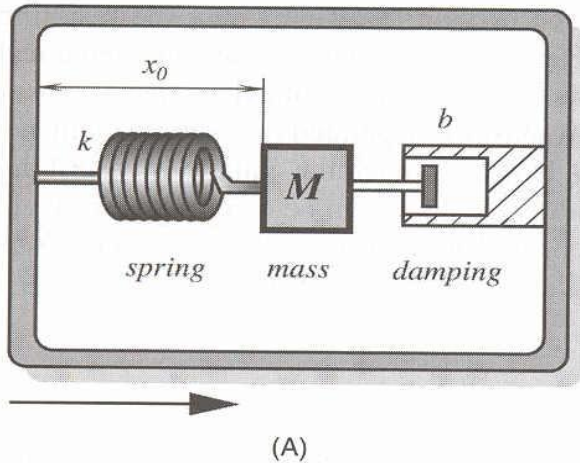
- Operate like metal resistive strain gauges
- Construction and properties are different.
- The gauge factor $\Delta R/(R\epsilon)$ much higher than for metals.
- Are typically smaller than metal types
- Often more sensitive to temperature variations (require temperature compensation).



4.1 Sensor Electronics

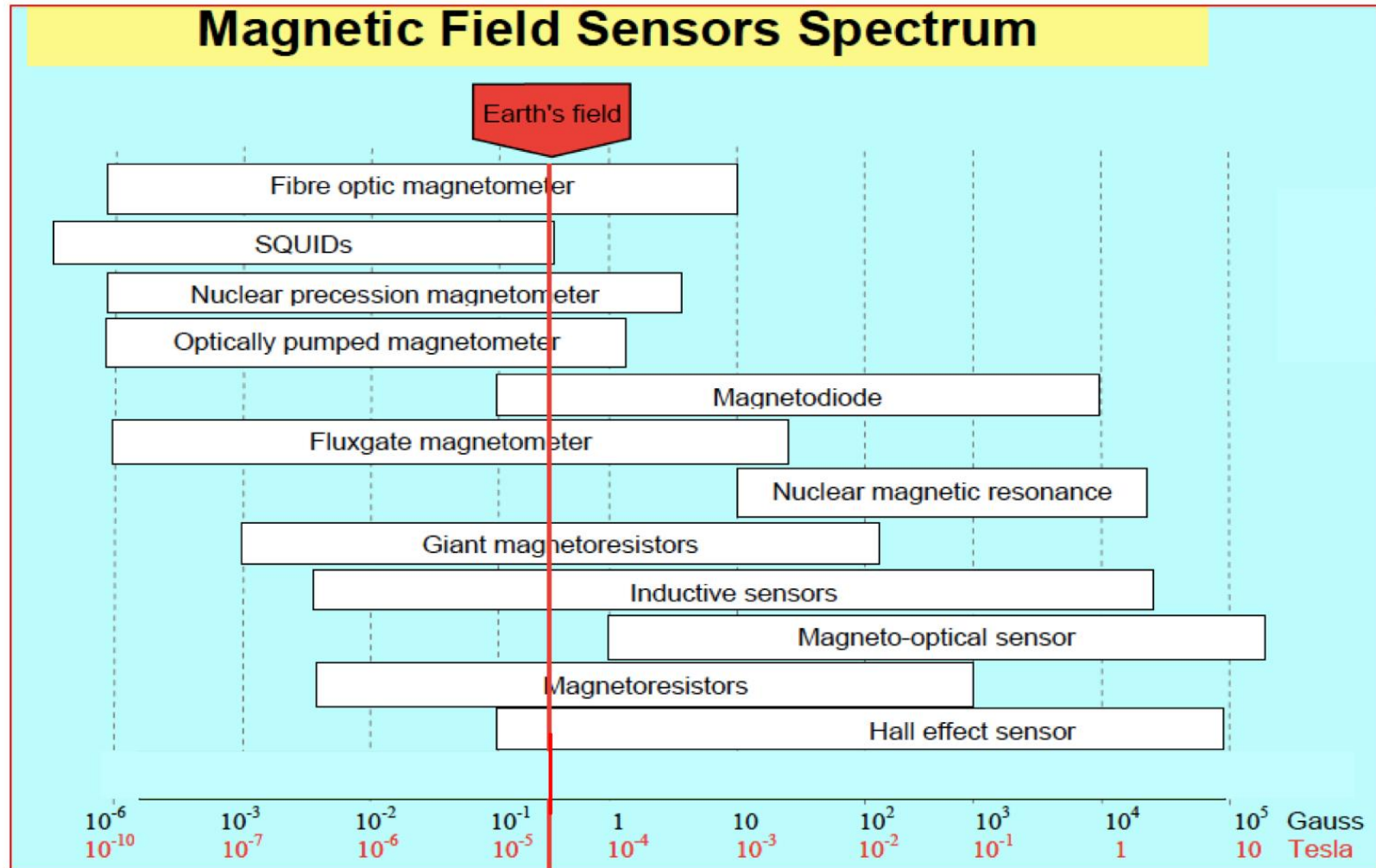
Accelerometers

- Newton's second law ($F = ma$) permit to sense acceleration by measuring the force on a mass.
- At any acceleration a , the force on the mass is directly proportional given a fixed mass.
- The strain gauge can perform the force measurement.



Capacitance proportional to vertical acceleration
Changes in capacitance are very small

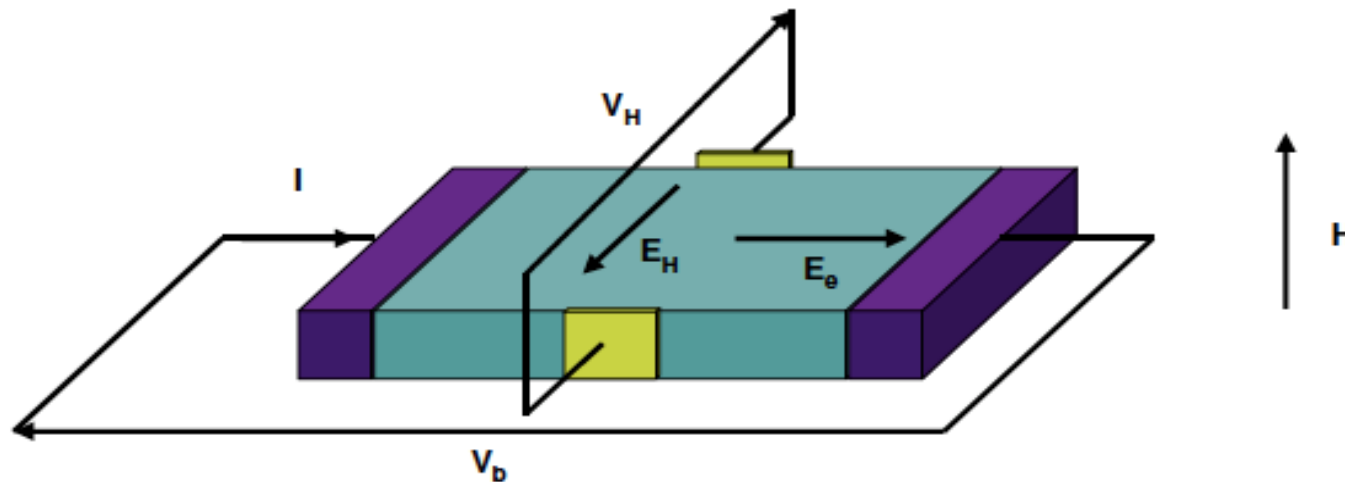
4.2 Magnetic Sensors



4.2 Magnetic Sensors

- Hall sensors

- A bias voltage V_b is applied to the plate via the two current contacts. The bias voltage creates an electric field E_e and forces a current I .
- If a perpendicular magnetic field H is applied to the device, a voltage appears between the sense contacts. This voltage V_H is called the **Hall voltage**.



4.2 Magnetic Sensors

- Hall sensors

- Hall voltage:

$$V_H = \frac{R_H}{t} I B_z = \frac{1}{nqt} I B_z$$

$R_H = 1/(nq)$ is the Hall constant, t the thickness of the plate, I the current, and B_z the projection of the magnetic field on the z axis.

- Sensitivity:

- The response of the output voltage of a Hall device to a magnetic field can be characterized by three figures of merit:

- the absolute sensitivity S_A : $S_A = \left| \frac{V_H}{B_z} \right|$

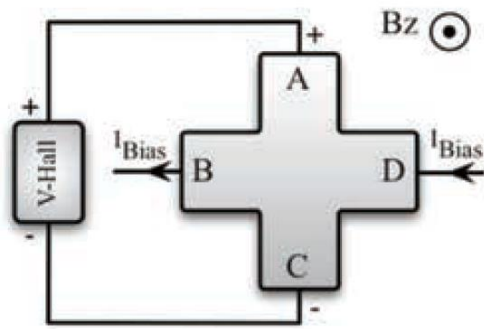
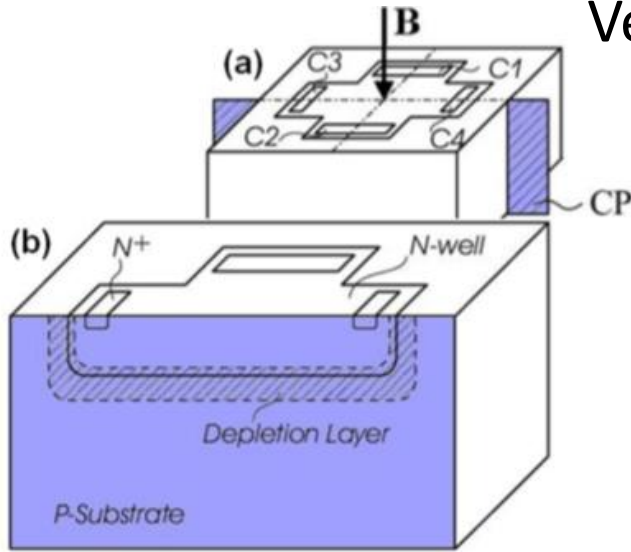
- the supply-current-related sensitivity S_I : $S_I = \frac{S_A}{I} = \left| \frac{1}{I} \frac{V_H}{B_z} \right|$

- and the supply-voltage-related sensitivity S_V : $S_V = \frac{S_A}{V} = \left| \frac{1}{V} \frac{V_H}{B_z} \right|$

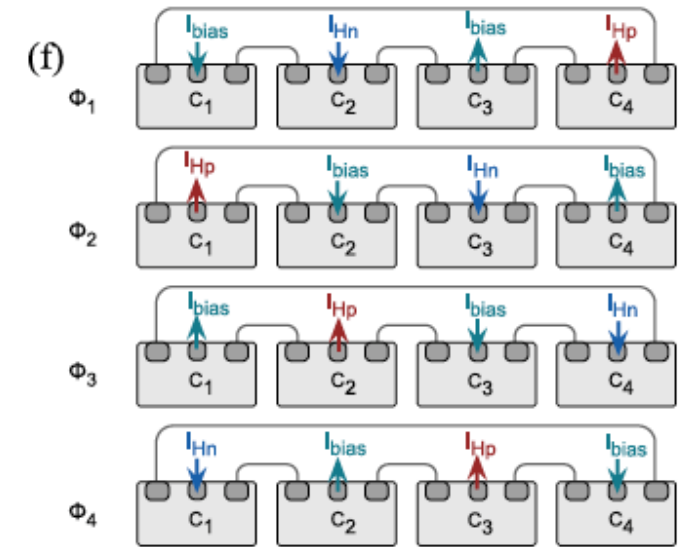
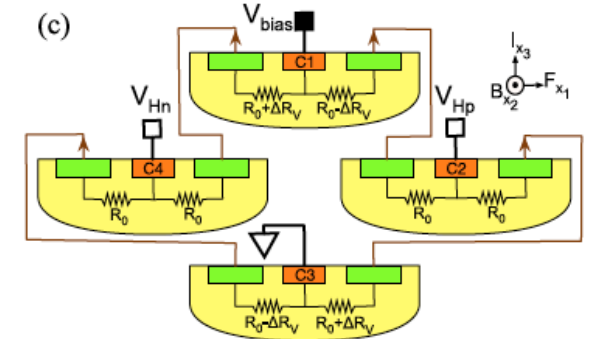
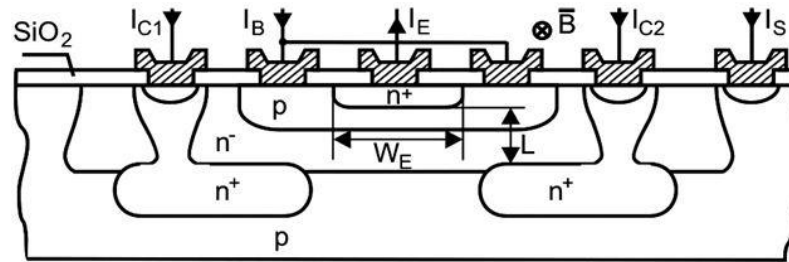
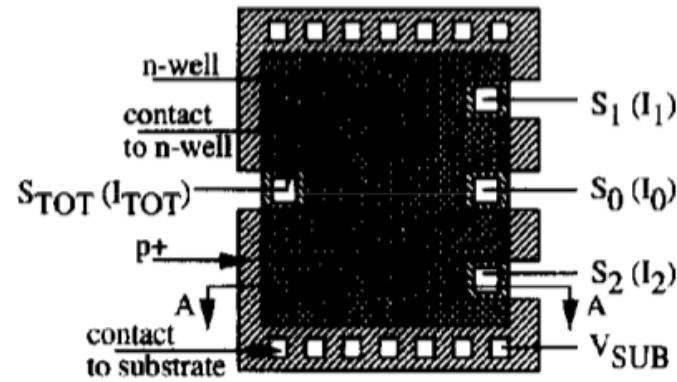
4.2 Magnetic Sensors

Hall devices

Vertical and horizontal sensitivity



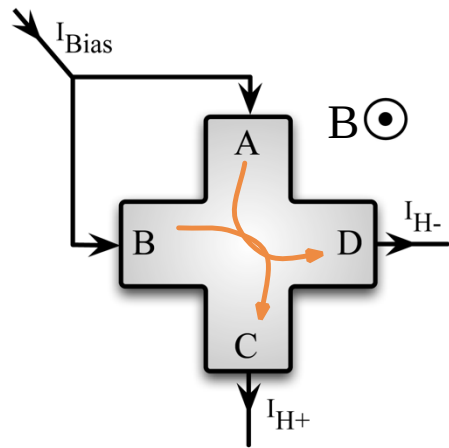
Spinning Current



Spinning Current

4.2 Magnetic Sensors

Current-Mode Hall Sensor

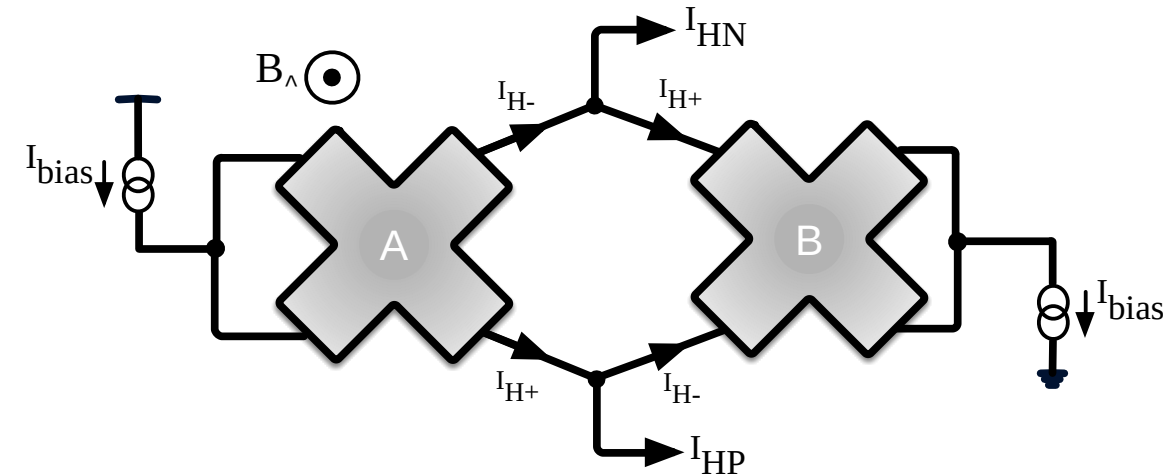


$$\text{Sensitivity } S_I = \frac{I_{Hall}}{I_{bias} B}$$

$$I_{H+} = \frac{I_{Bias}}{2} + \frac{I_{Hall}}{2}$$

$$I_{H-} = \frac{I_{Bias}}{2} - \frac{I_{Hall}}{2}$$

Twin Current-Mode Hall Sensor

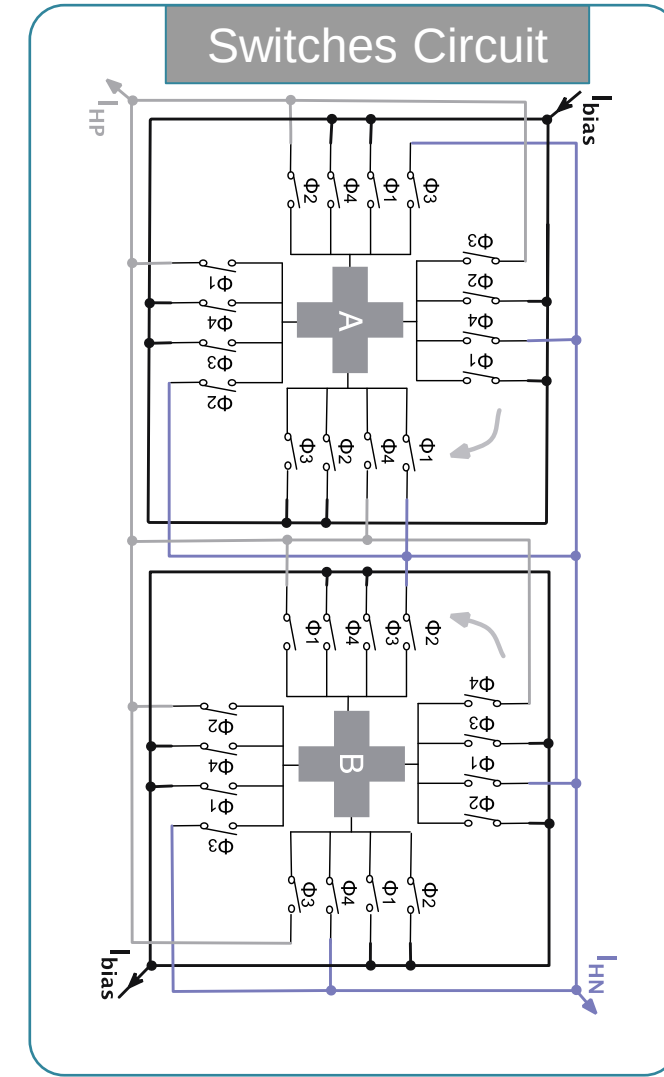
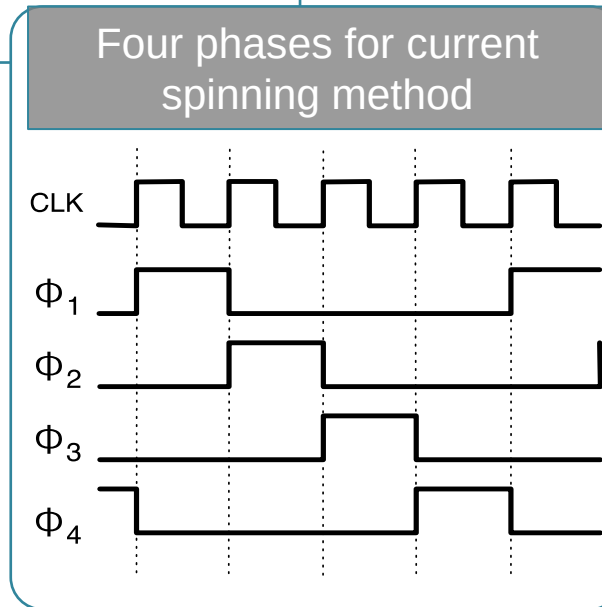
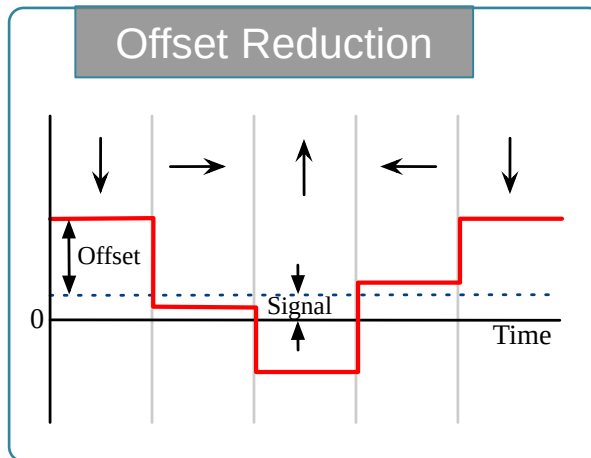
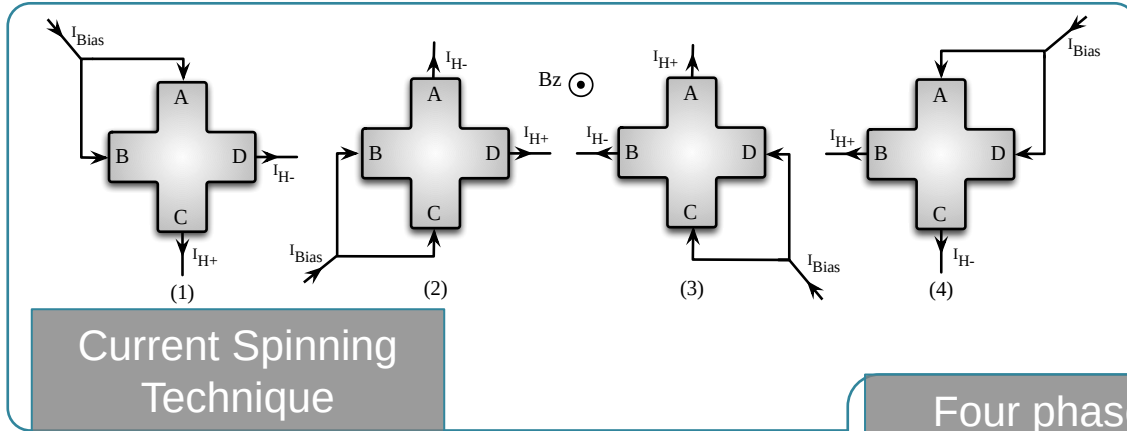


$$I_{HP} = I_{H+} - I_{H-} = I_{Hall}$$

$$I_{HN} = I_{H-} - I_{H+} = -I_{Hall}$$

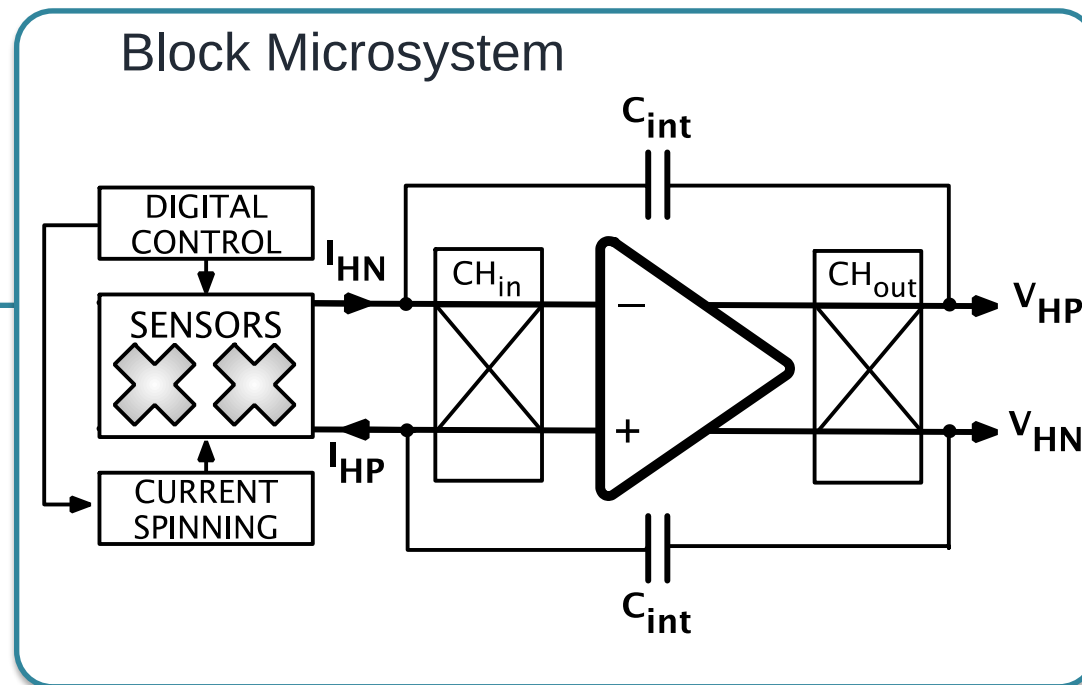
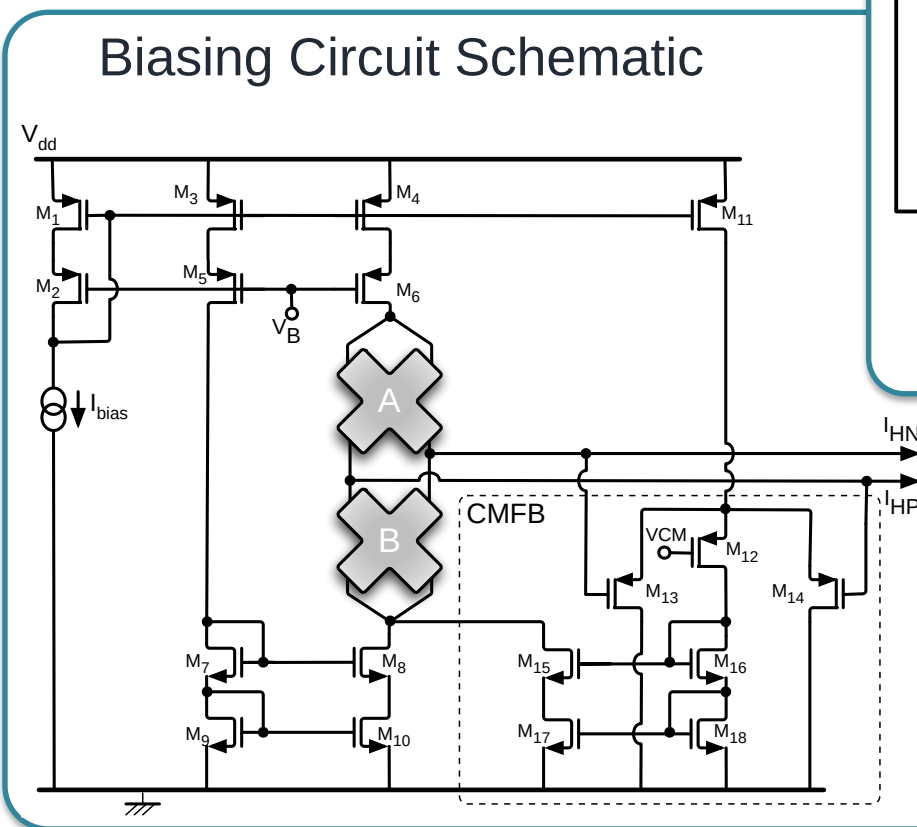
4.2 Magnetic Sensors

OFFSET REDUCTION



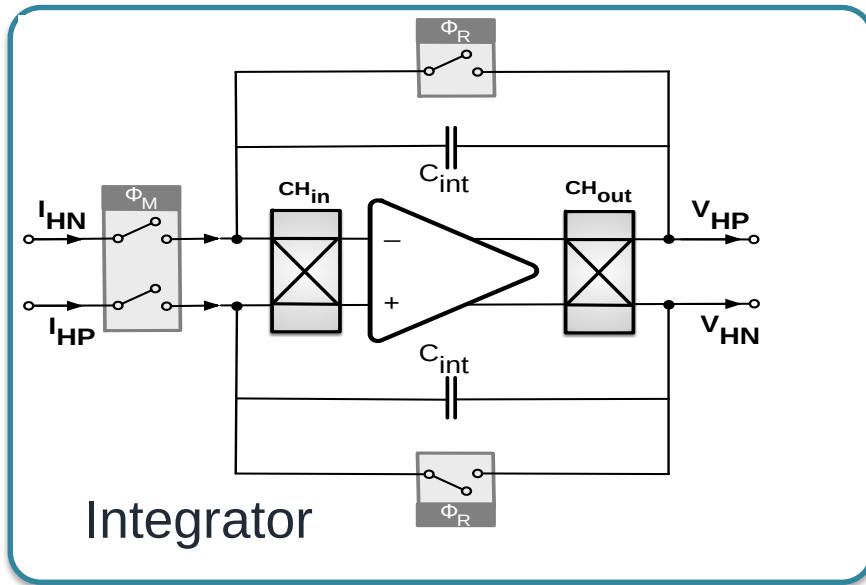
4.2 Magnetic Sensors

Implementation of Hall Plate Sensors and Relevant Switches and Biasing Circuit



The **two current generators** are nominally equal. The CMFB corrects mismatch.

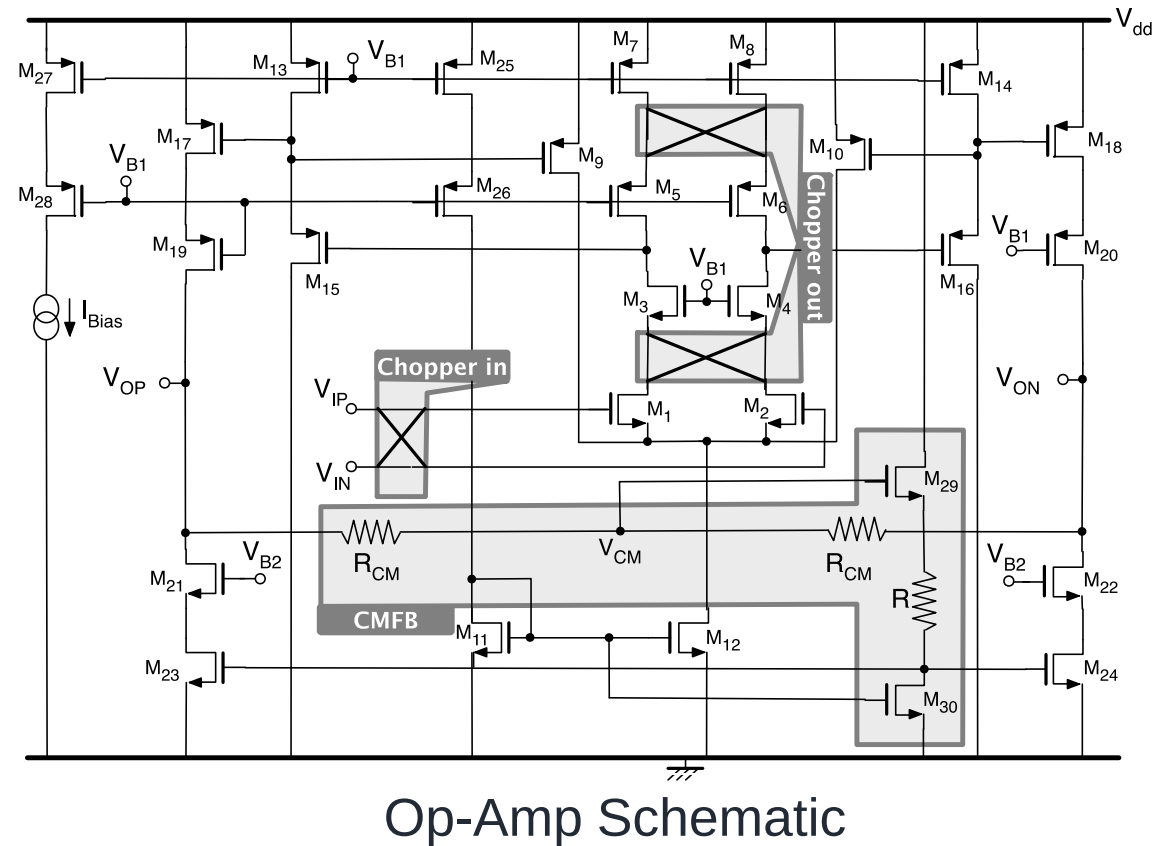
4.2 Magnetic Sensors



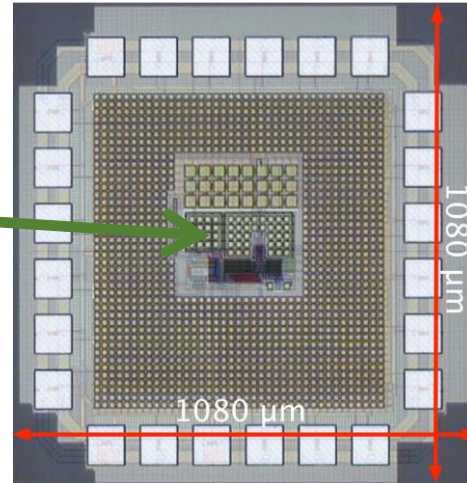
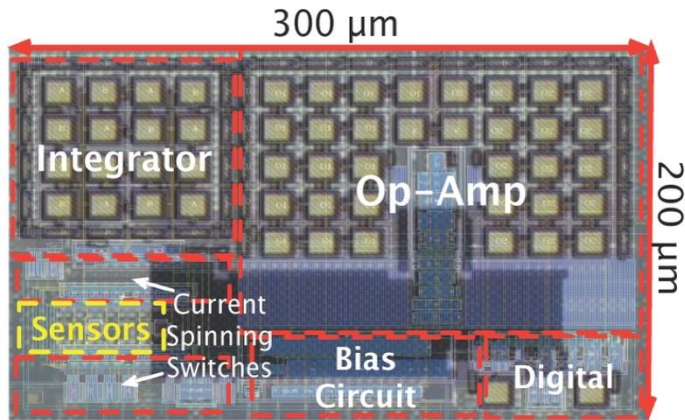
READOUT PERFORMANCE SUMMARY

Technology	0.18 μm
Supply Voltage	1.8 V
DC GAIN	109 dB
GBW	10 MHz
Phase Margin	60 Degree
Power Consumption	54 μW
Load Cap	2 pF
Output Range	1.2 V

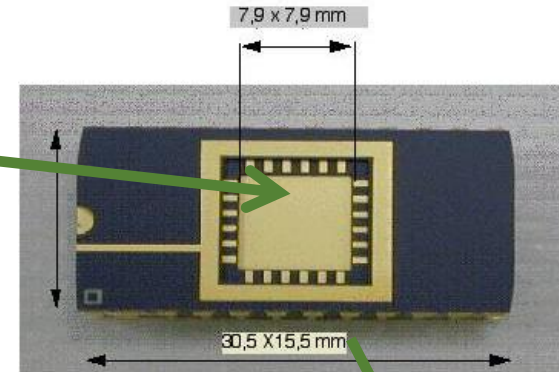
Implementation of integrator
readout circuit in a 0.18 μm
CMOS technology



4.2 Magnetic Sensors



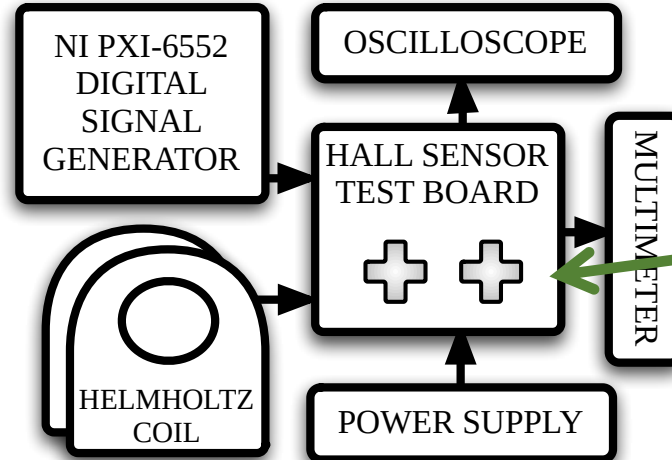
DIL 24-pin package



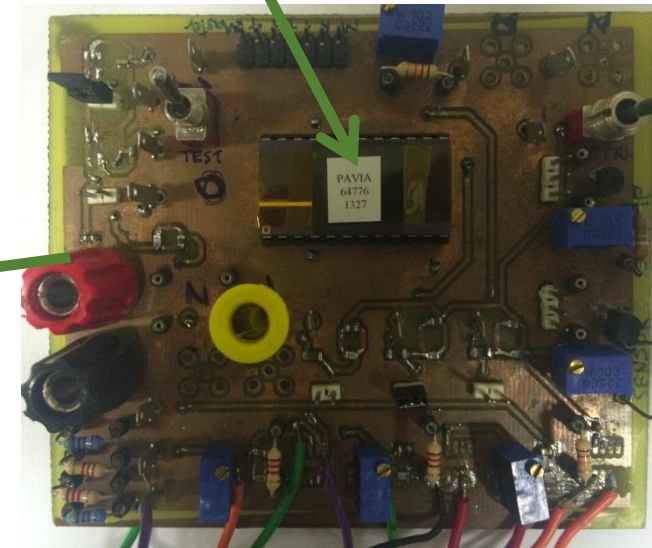
H. Heidari, E. Bonizzoni, U. Gatti, and F. Maloberti, "A CMOS Current-Mode Magnetic Hall Sensor with Integrated Front-End", IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 62, Issue: 5, pp. 1270-1278, May 2015.

MICROSYSTEM PERFORMANCE

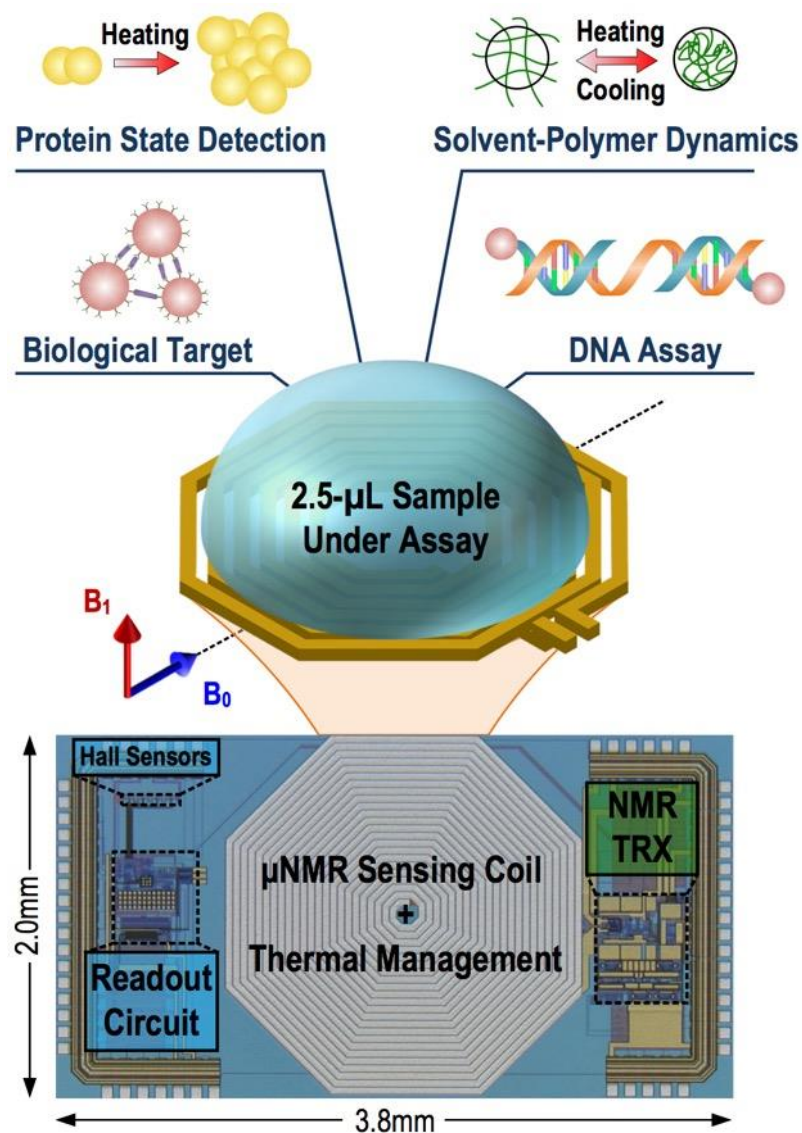
Sensitivity	1660 V/A/mT	
Offset	50 μT	
Range	0 ~ 10 mT	
Sensors	2 Plate	
Sensor Size	$8 \times 8 \mu\text{m}^2$	
Nonlinearity	$< \pm 0.2 [\%_{\text{FS}}]$	
Switches	$80 \times 50 \mu\text{m}^2$	
Power Consumption	Sensor	65 μW
	Integrator	54 μW



Measurement Set-up

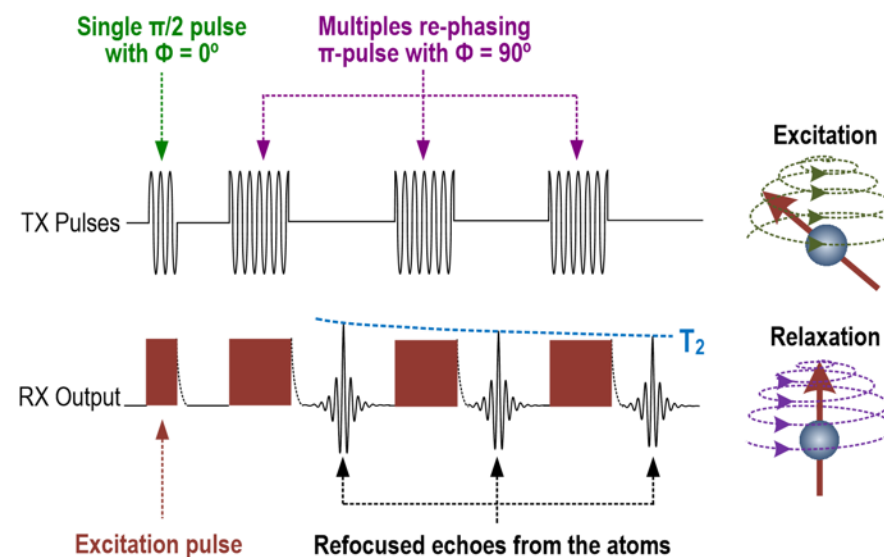


4.2 Magnetic Sensors



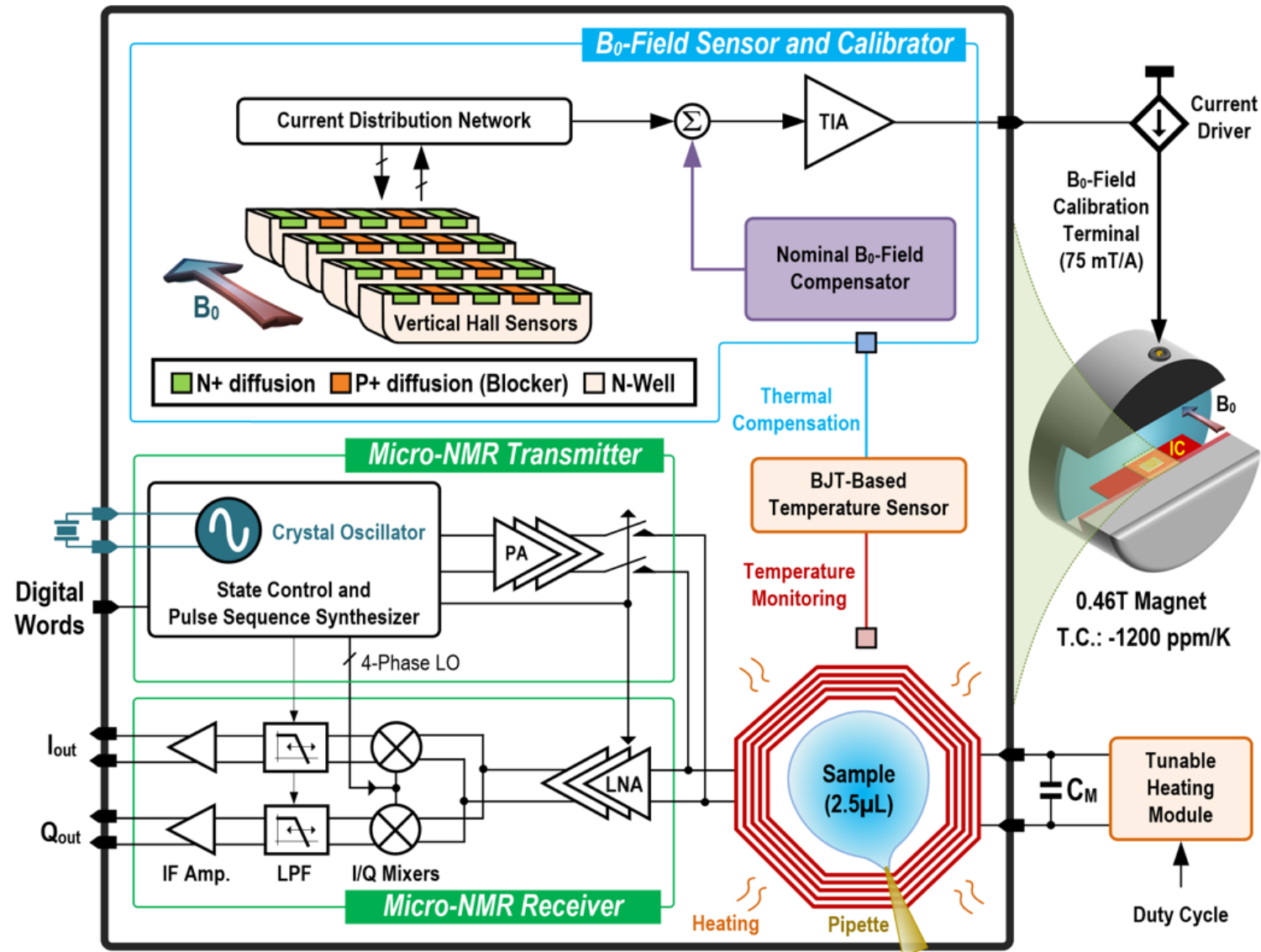
MAGNETIC SENSOR FOR μNMR

CMOS-based Magnetic Resonance Spectroscopy in a 0.18 μm CMOS technology

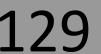


K.-M. Lei, H. Heidari, P.-I. Mak, M.-K. Law, F. Maloberti, R.P. Martins, "A handheld 50pM-sensitivity micro-NMR CMOS platform with B-field stabilization for multi-type biological/chemical assays", IEEE International Solid-State Circuits Conference (ISSCC) Dig. Tech. Pap., pp. 474-475, Feb. 2016.

4.2 Magnetic Sensors

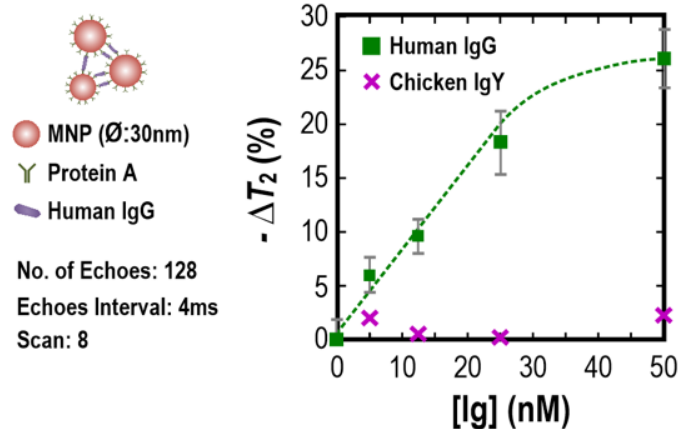


ÉCOLE POLYTECHNIQUE
FÉDÉRALE DE LAUSANNE



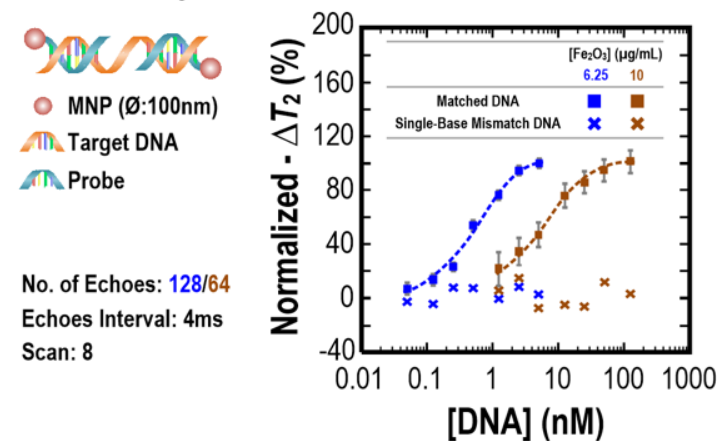
4.2 Magnetic Sensors

Immunoglobulin G



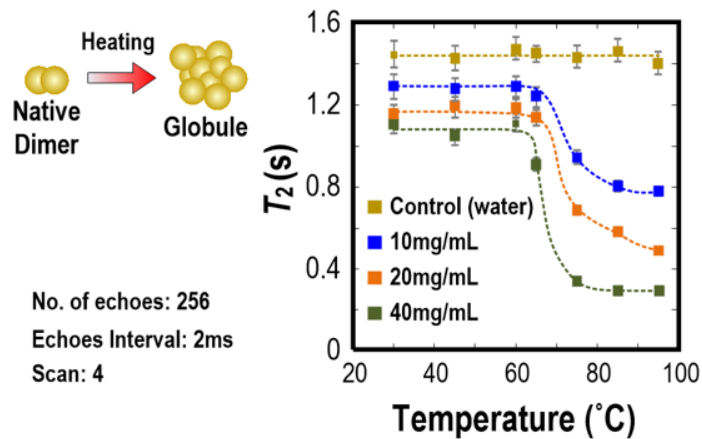
(a)

E. faecalis derived DNA



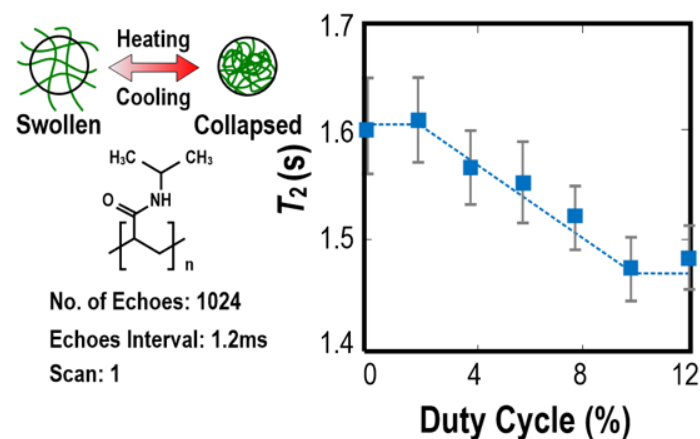
(b)

β-lactoglobulin



(c)

Poly(N-isopropylacrylamide)



(d)

4.3 Offset compensation

Why?

Often electronic systems must interface signals:

- **whose information is close to DC**
- **and is in the millivolt range**

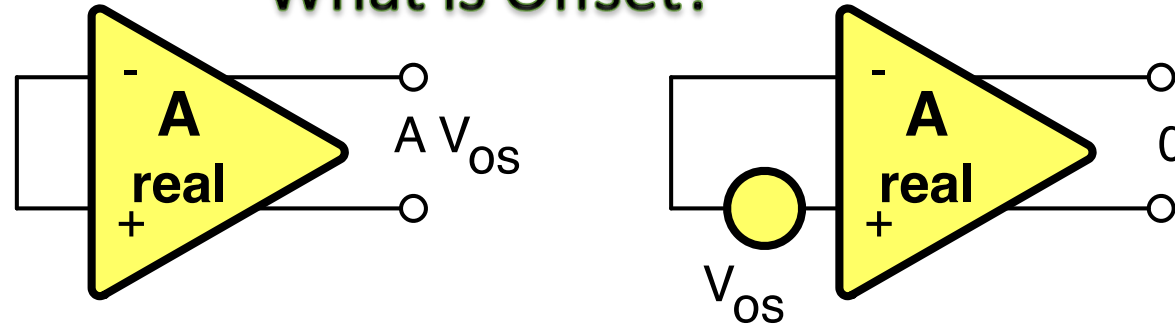
AC interfacing is
not a good idea

the offset level of standard IC
amplifier, especially in CMOS

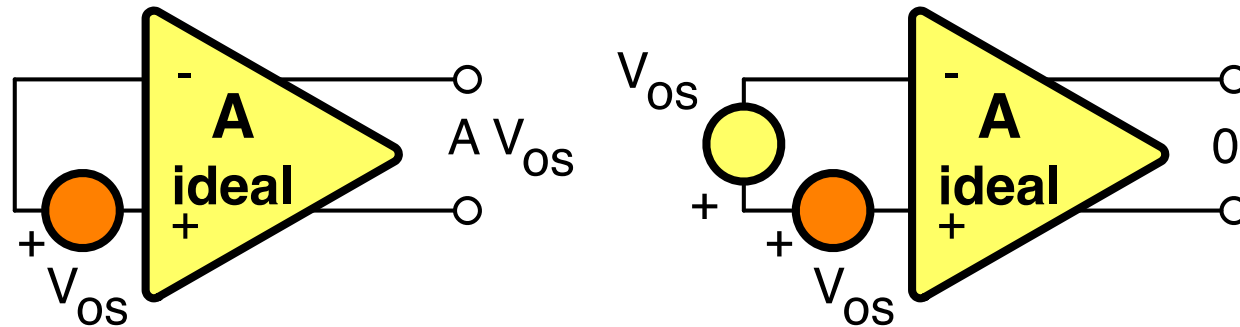
Many sensor systems (temperature, pressure, humidity, gas concentration, Hall, ...) belong to this category

4.3 Offset compensation

What is Offset?



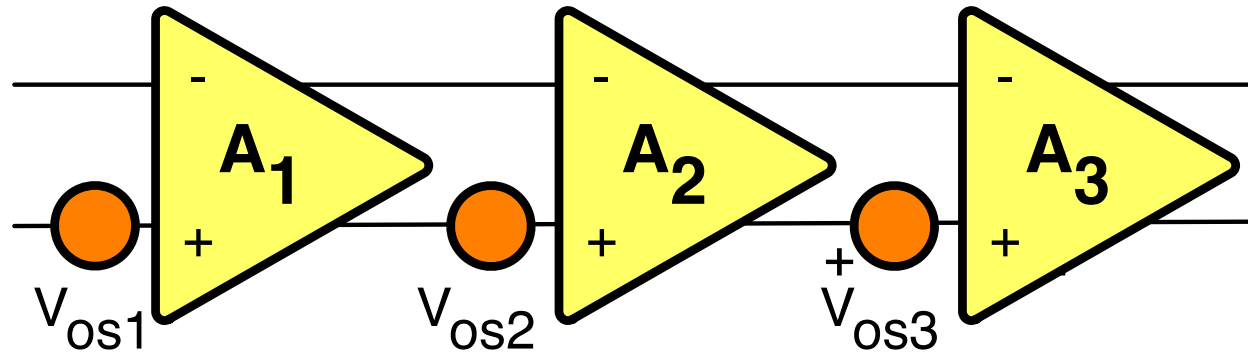
Offset is the compensation signal to be applied at the input of a system to make its output equal to zero



Offset can be modeled with a voltage source at the input

4.3 Offset compensation

CASCADE OF GAIN STAGES



$$V_{os} = \sum_{i=1}^k \frac{V_{os,i} + V_{aging,i}}{\prod_{j=2}^i A_j}.$$

$$V_{os,i} = V_{os0,i} [1 + T_C \Delta T + PSRR \cdot \Delta V_{dd} + CMRR \cdot \Delta V_{cm}]$$

Pelgrom, M.J.M.; Duinmaijer, A.C.J.; Welbers, A.P.G.; "Matching properties of MOS transistors",
IEEE Journal of SSC, vol.24, no.5, pp.1433-1439, Oct 1989.

4.3 Offset compensation

Offset is not a constant signal...

Offset changes with time! It drifts with:

- Temperature $\rightarrow T_C V_{os}$
- Voltage Supply $\rightarrow PSRR$
- Input Level $\rightarrow CMRR$
- Ageing $\rightarrow$ Long Term Stability

Moreover also offset caused by packaging stress

$$T_C \sim 10\mu V/^{\circ}C$$

$$PSRR \sim 80dB$$

$$CMRR \sim 80dB$$

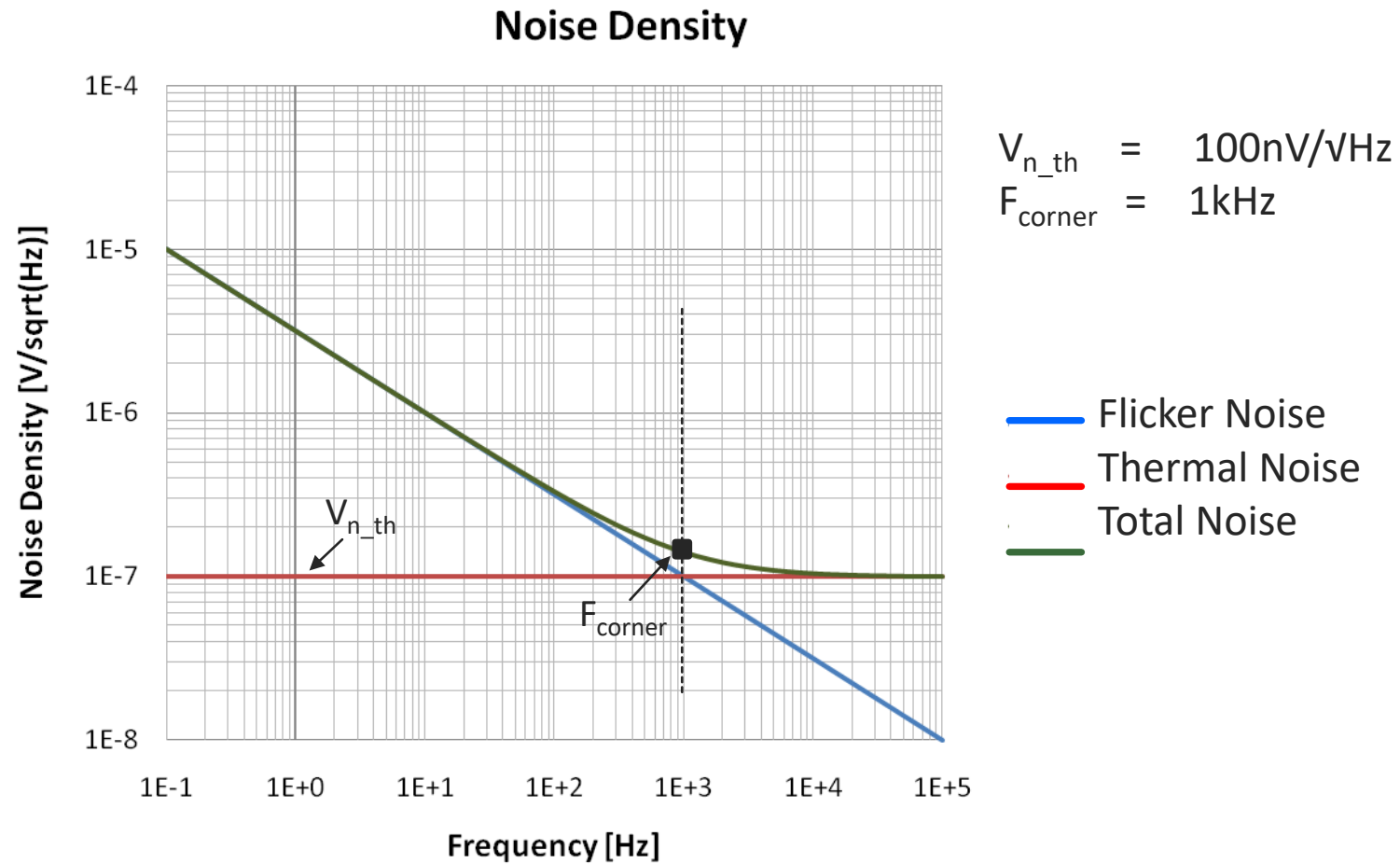
$$\Delta T = 60^{\circ} \quad \underline{600}\mu V$$

$$\Delta V = 1V \quad \underline{100}\mu V$$

Static methods compensate for offset at given operating conditions.

4.3 Offset compensation

In addition there is the Noise



Dynamic Offset Compensation

Techniques that use electronic circuits to compensate for the offset during the operational amplifier operation.

- More effective than trimming
- Can require a specific time-slot for compensation
- Can give rise to unwanted spur near the signal band
- Cost to pay: more complex circuitry

4.3 Offset compensation

Dynamic Offset Compensation Techniques

Autozeroing
(mainly for comparators)

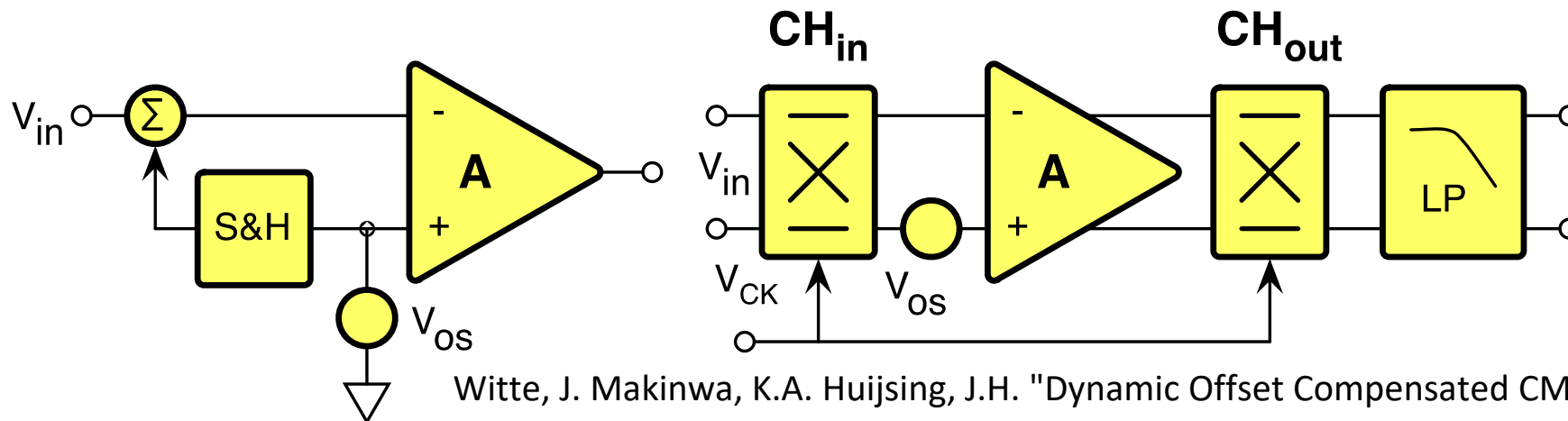


Measure the offset and correct it

Chopping



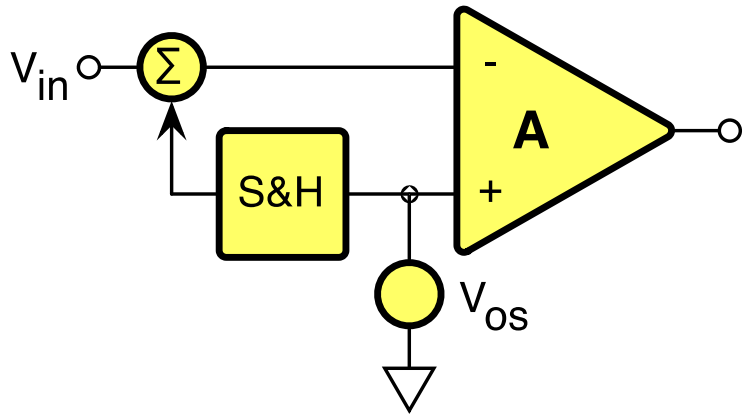
Exploit a modulation technique to process offset and signal in different ways



Witte, J. Makinwa, K.A. Huijsing, J.H. "Dynamic Offset Compensated CMOS Amplifiers", Springer, 2009

4.3 Offset compensation

Autozero in the Time Domain



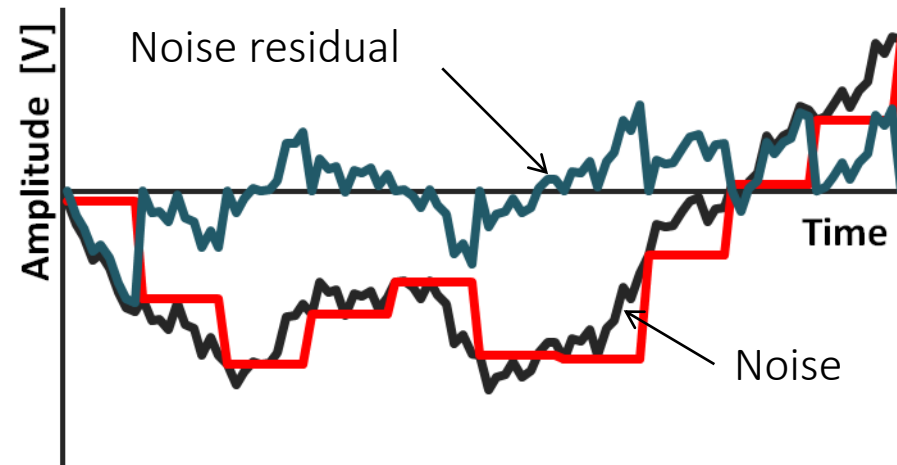
Noise



Slow components eliminated



Fast components superposed

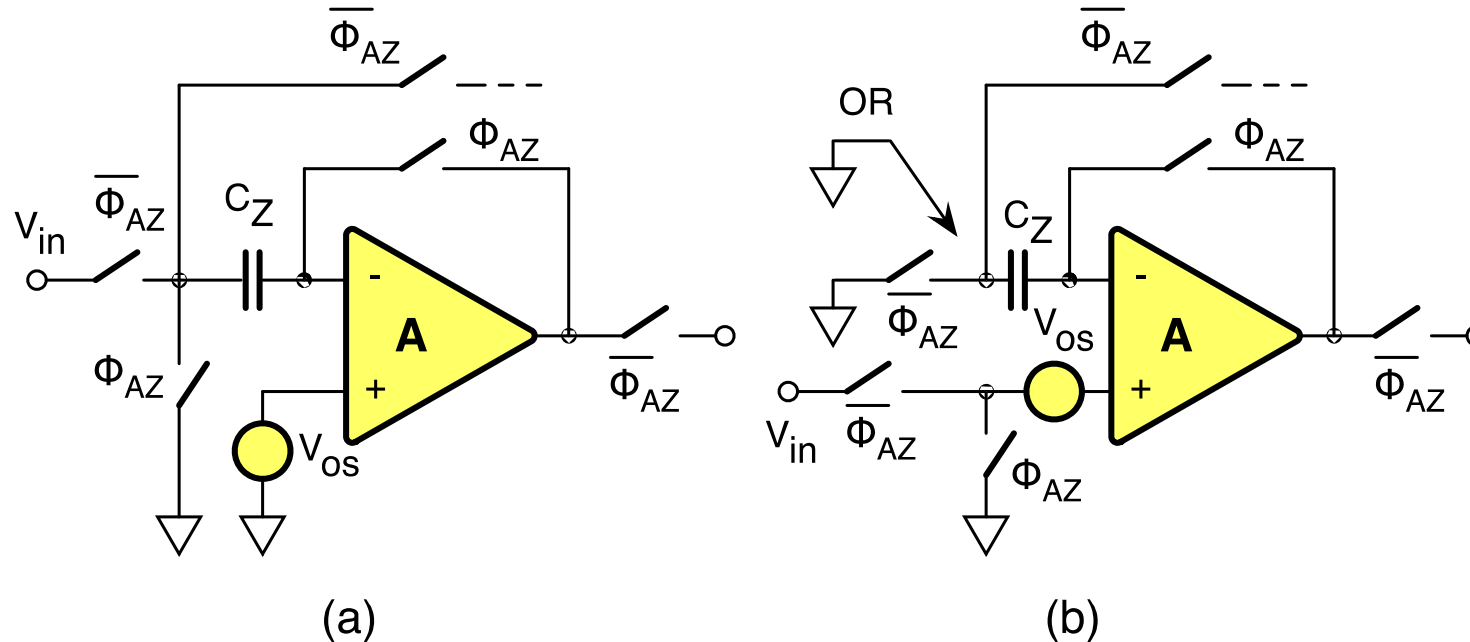


Storage at input
Storage at output
Storage with aux stage

Enz, C.C.; Temes, G.C.; "Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization" *Proc. IEEE*, pp.1584-1614, 1996

4.3 Offset compensation

Autozero (Storage at Input)



Not a continuous time operation

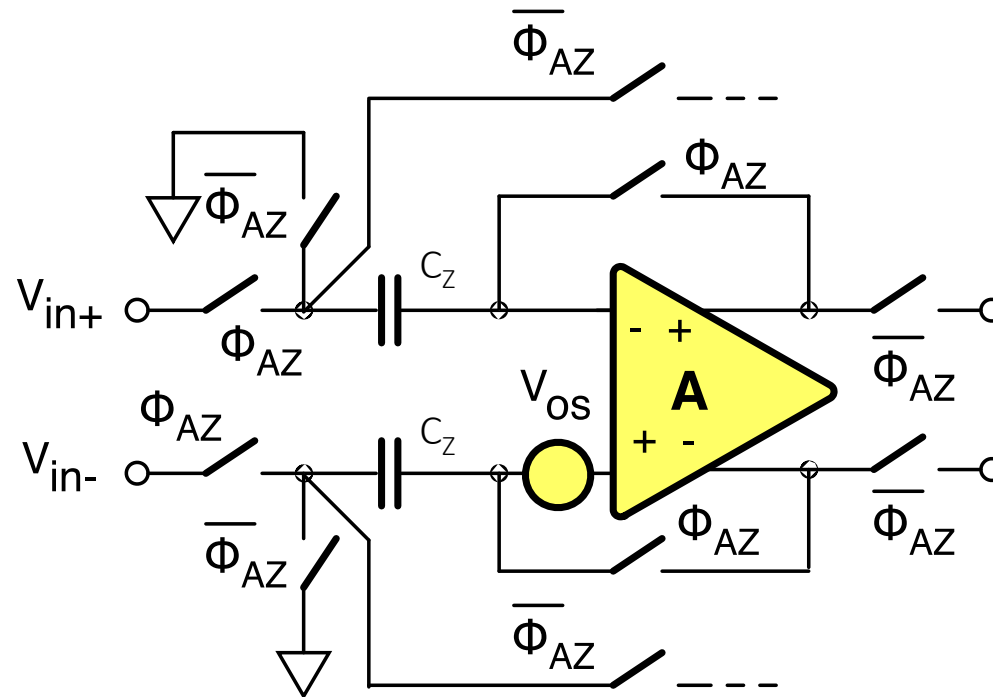
☹️ Unity gain stability required

There is a residual offset caused by

- Finite gain: the unity gain configuration does not give rise to V_{OS} at the input but $\sim V_{OS} (1-1/A)$
- Charge injection: opening the switch injects charge into C_Z

4.3 Offset compensation

Fully Differential Autozero (Storage at Input)

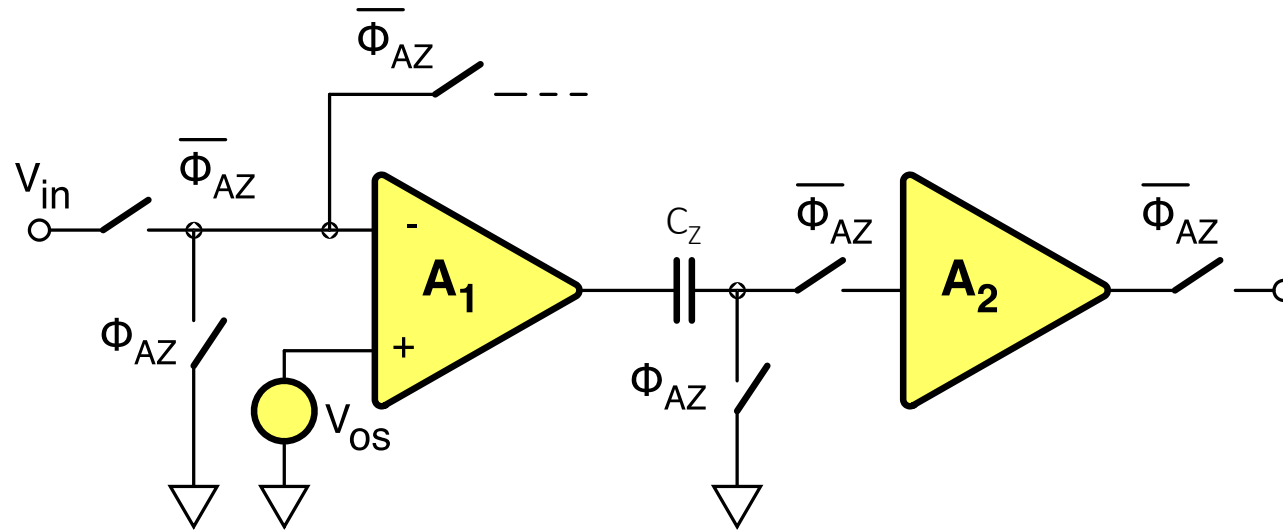


$$V_{OS,res} \gg \frac{V_{OS}}{A+1} + \frac{q_{inj}}{C_Z} \frac{dq_{inj}}{dq_{inj}} + \frac{dC_Z}{C_Z} \frac{U}{U}$$

Differential circuits are less sensitive to charge injection.
The charge injection **mismatch** and cap **mismatch** matter

4.3 Offset compensation

Autozero (Storage at Output)

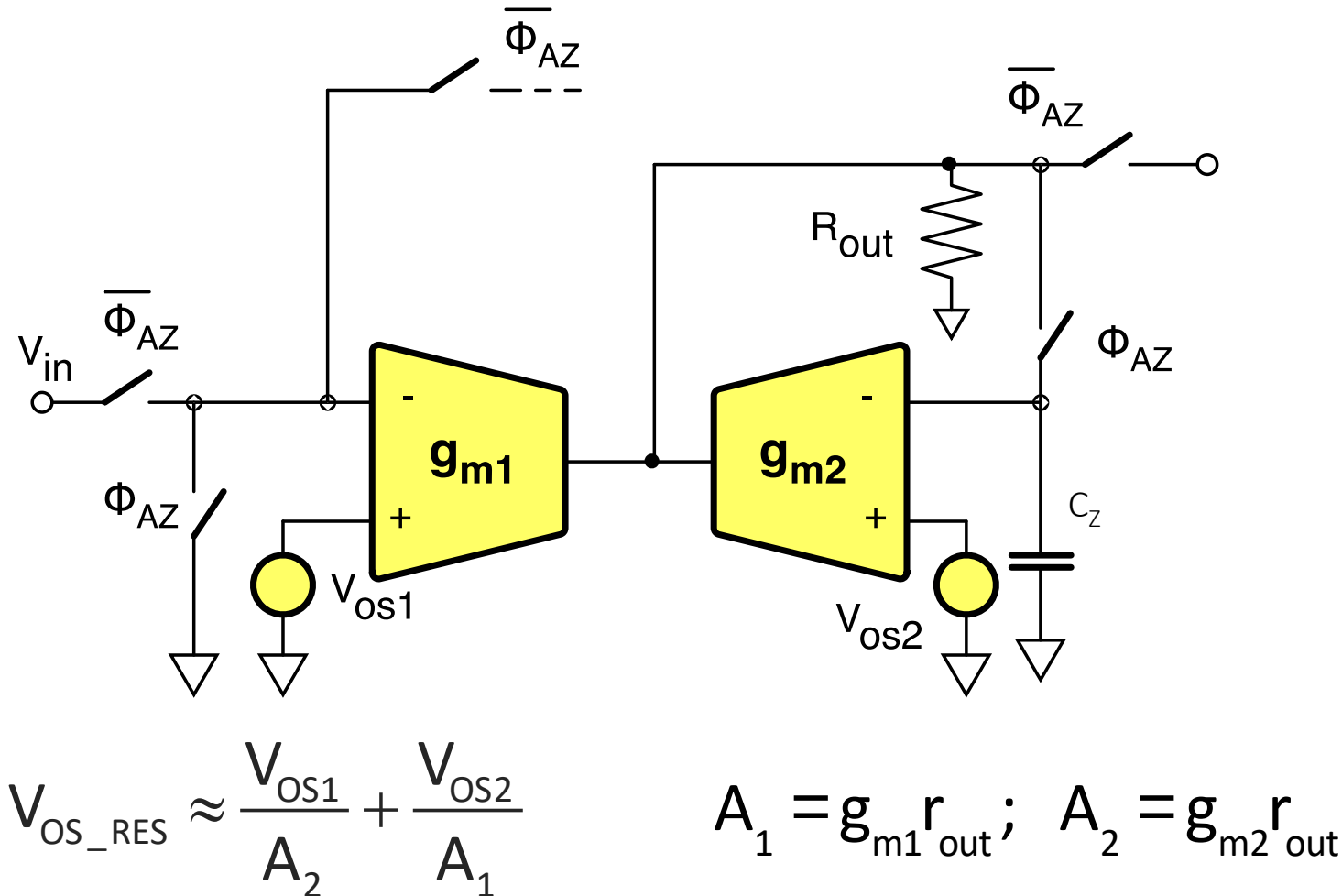


- ☺ Unity gain stability not required
- ☺ No residual offset due to finite gain
- ☺ Residual offset caused only by charge injection
- ☹ Gain is limited because dynamic range is reduced by AV_{OS}

$$V_{OS_RES} \gg \frac{q_{inj,tot}}{A_1 C_Z}$$

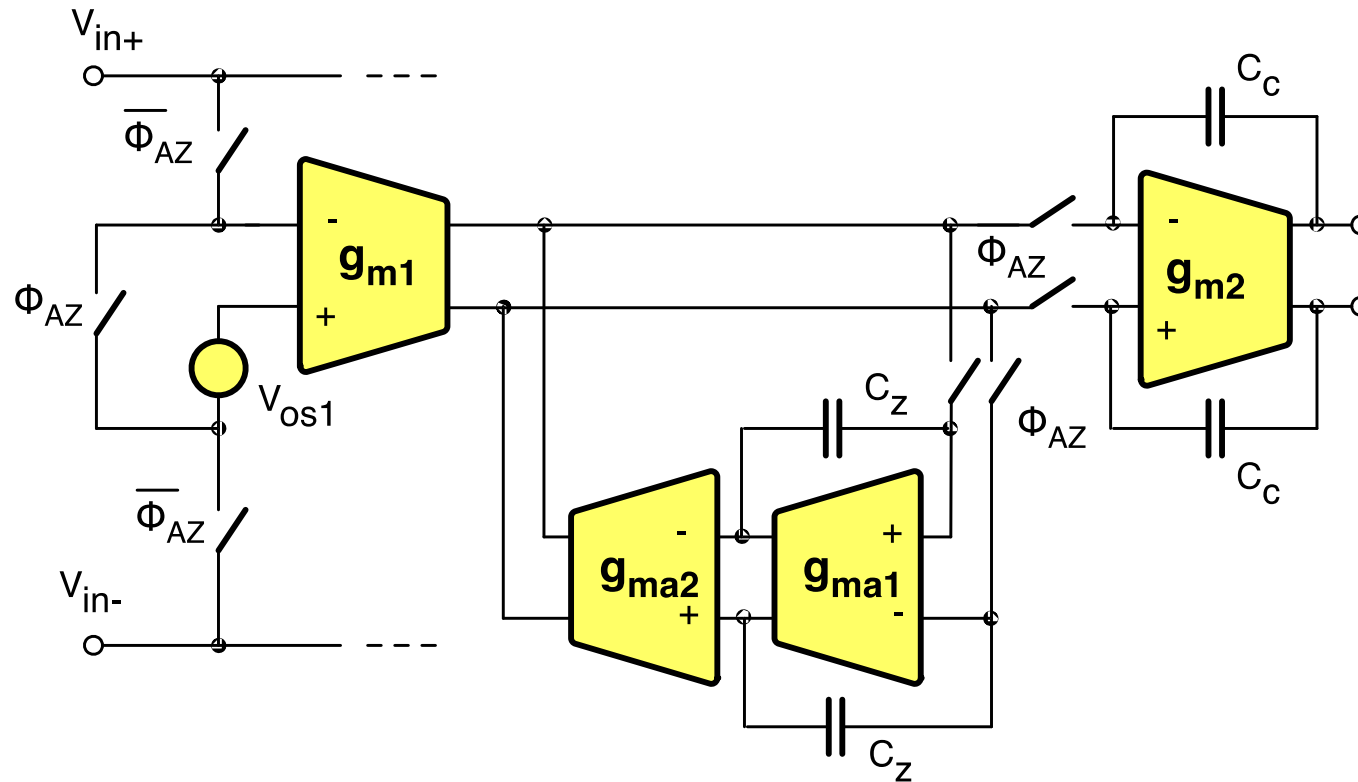
4.3 Offset compensation

Autozero (Storage in Auxiliary Stage - AOS)



4.3 Offset compensation

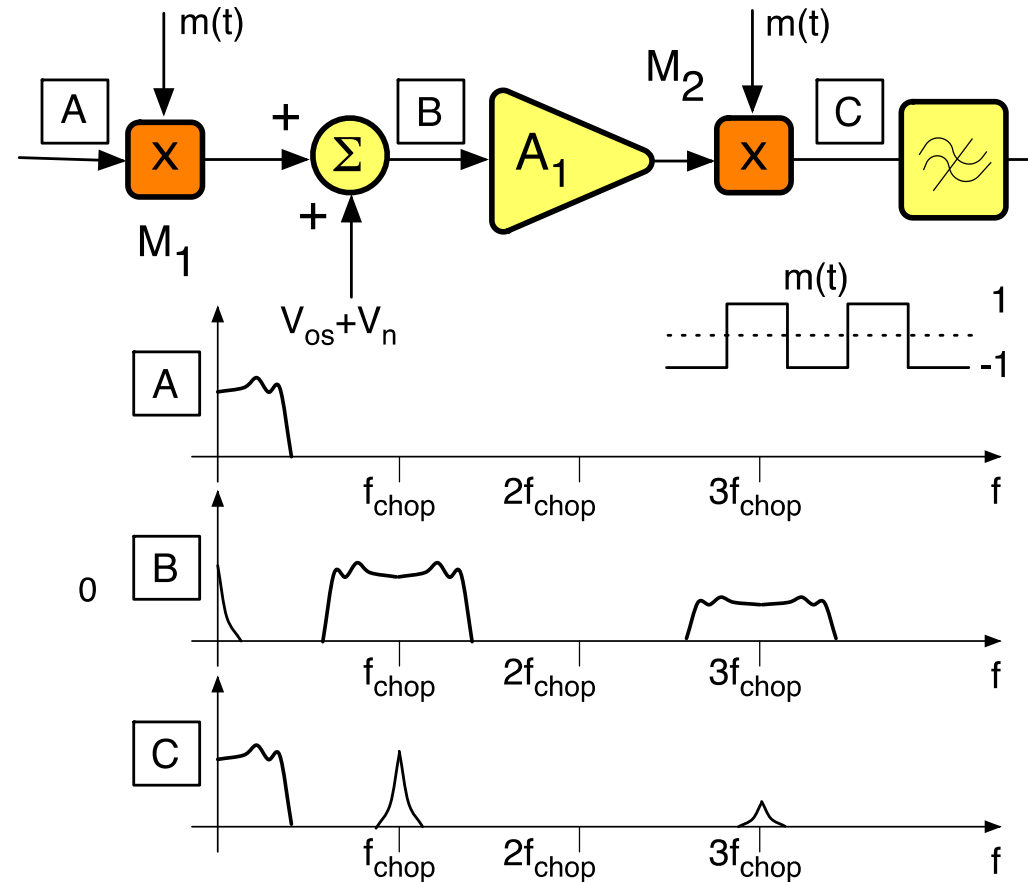
Autozero (Storage in Auxiliary Stage - AOS)



Use of active integrator to compensate for the amplified offset on feedback elements.
Offset of the auxiliary stage in the residual term

4.3 Offset compensation

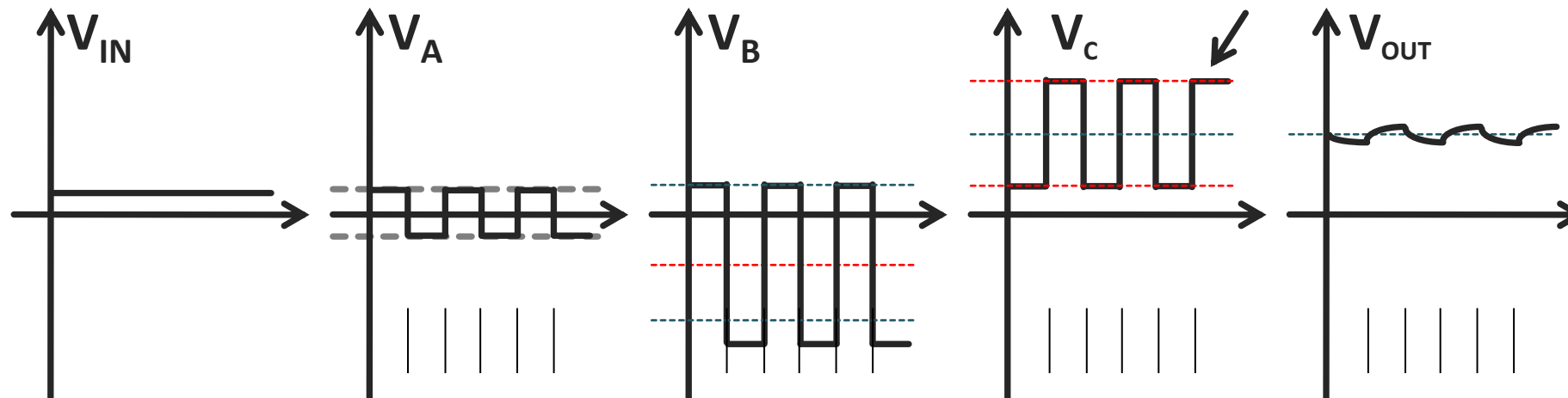
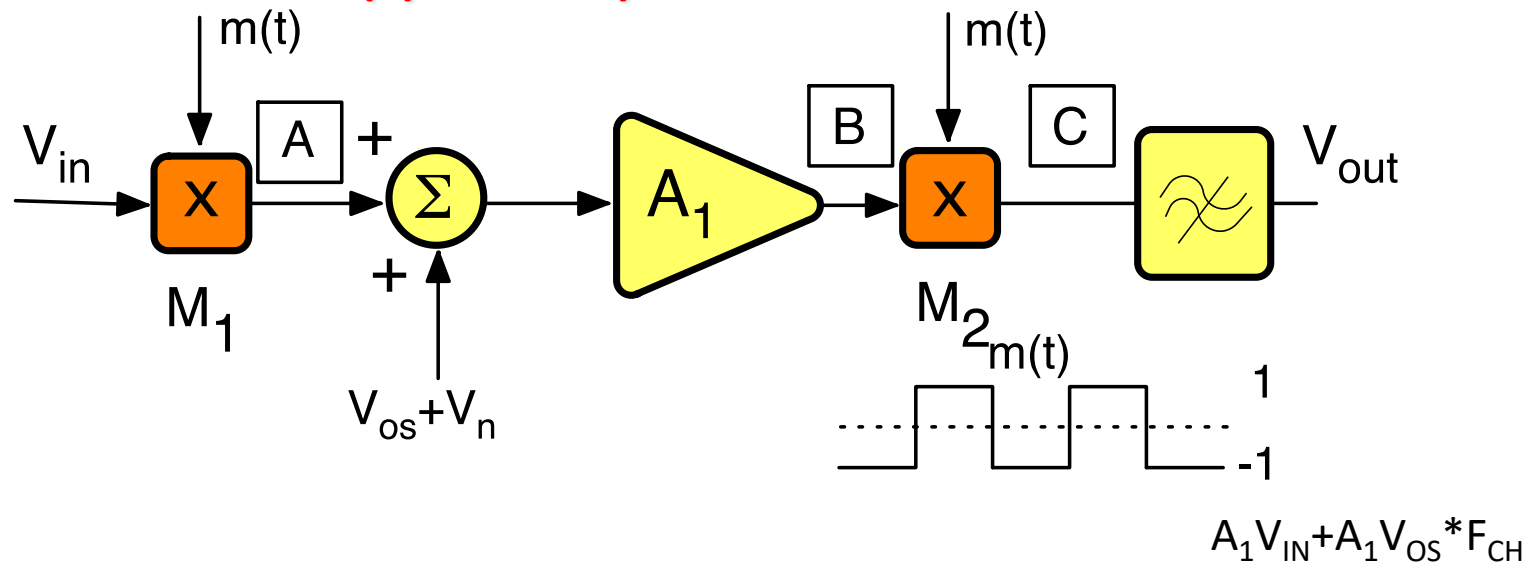
Chopper Amplifier in the frequency domain



Enz, C. C.; Vittoz, E. A.; Krummenacher F.; "A CMOS chopper amplifier, *IEEE JSSC*, pp.335-342, 1987

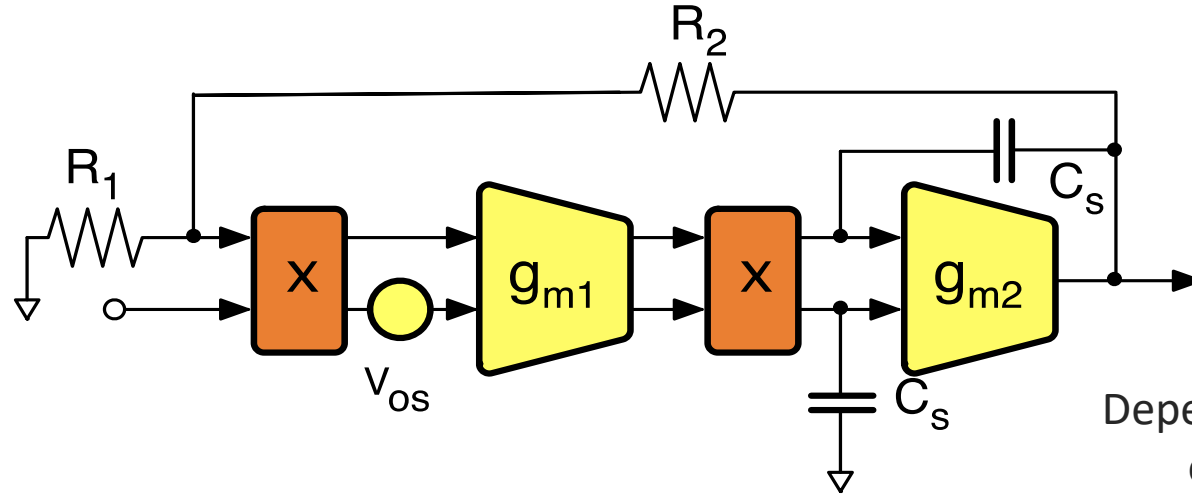
4.3 Offset compensation

Chopper Amplifier in the time domain

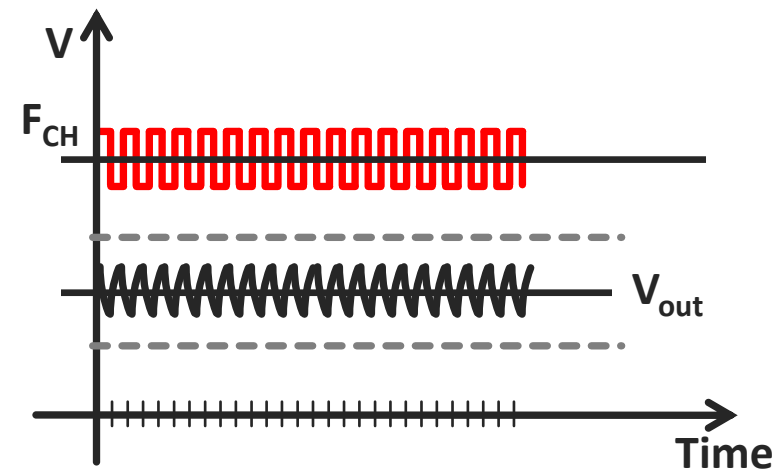
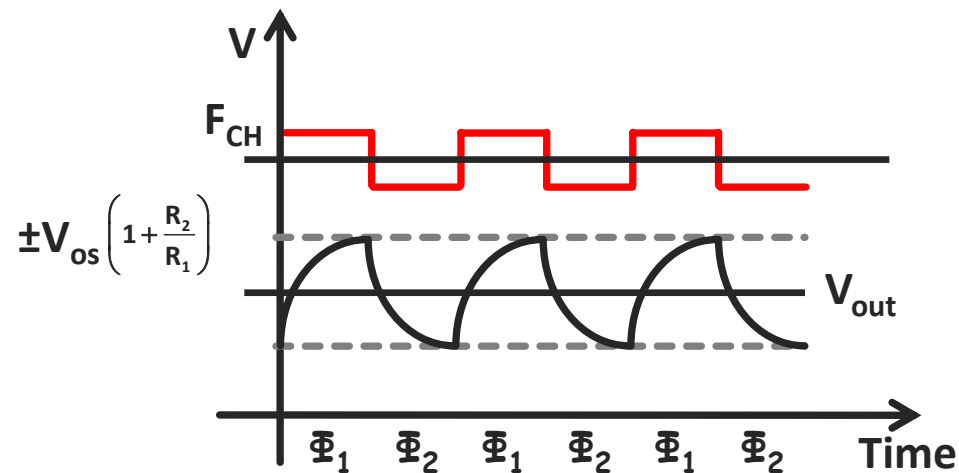


4.3 Offset compensation

Chopper Amplifier in the time domain



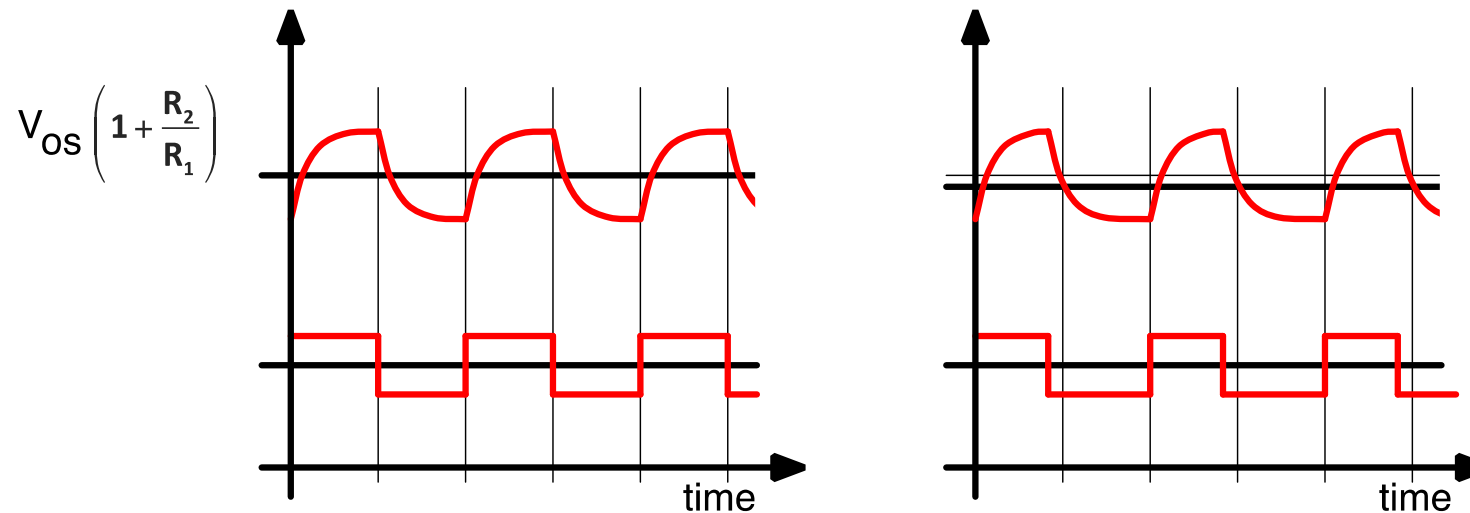
Depending on f_{CK} the ripple reaches or not the asymptotic value



4.3 Offset compensation

LIMIT: Residual Offset

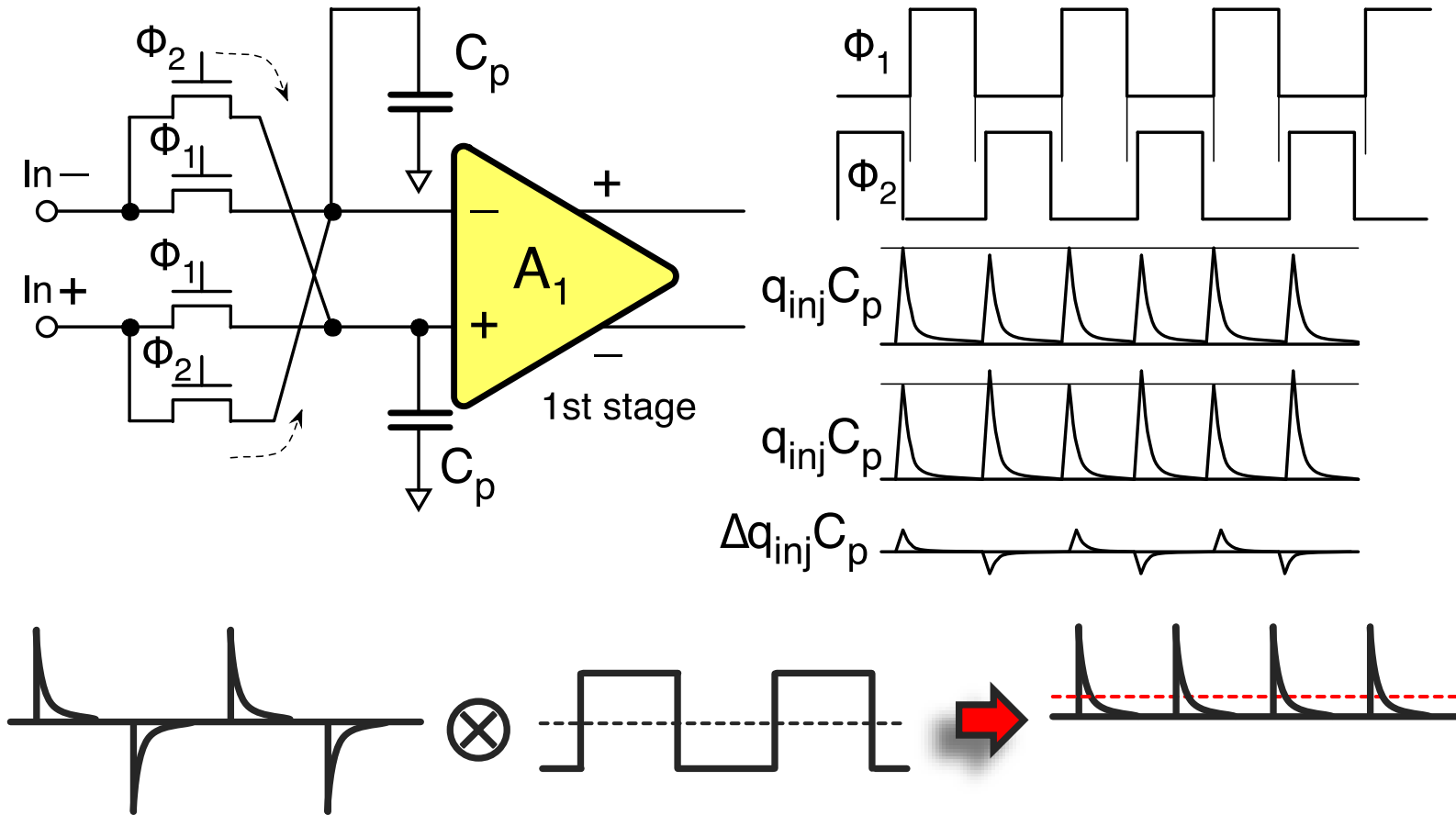
- Second stage offset (divided by the first stage gain)
- Clock duty cycle not at 50%
- Charge injection **mismatch** demodulation



4.3 Offset compensation

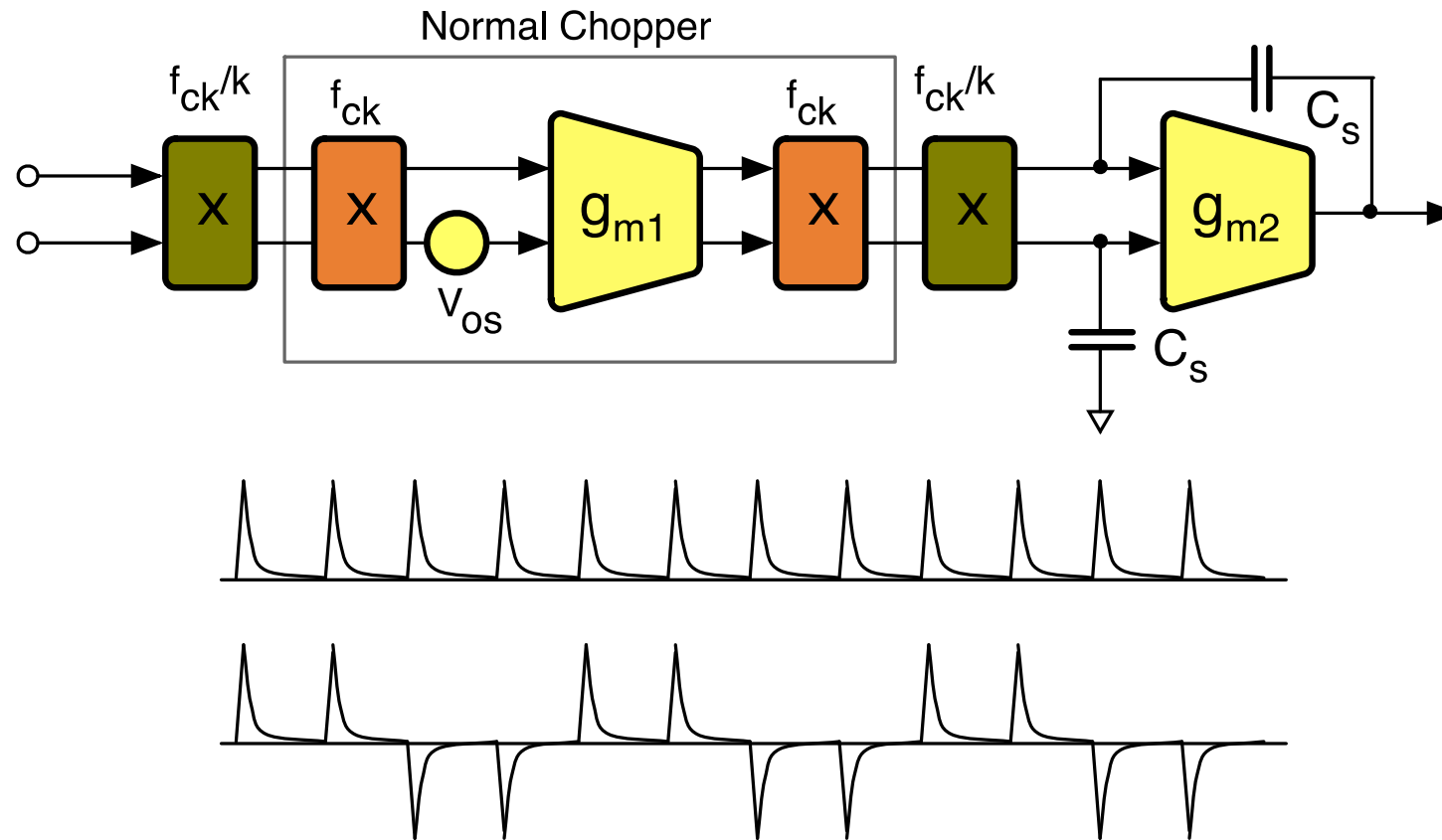
LIMIT: Residual Offset

- Charge injection **mismatch** plus demodulation



4.3 Offset compensation

REMEDY: Nested Chopper



- Second demodulation makes zero the average of the the charge injection **mismatch**

4.3 Offset compensation

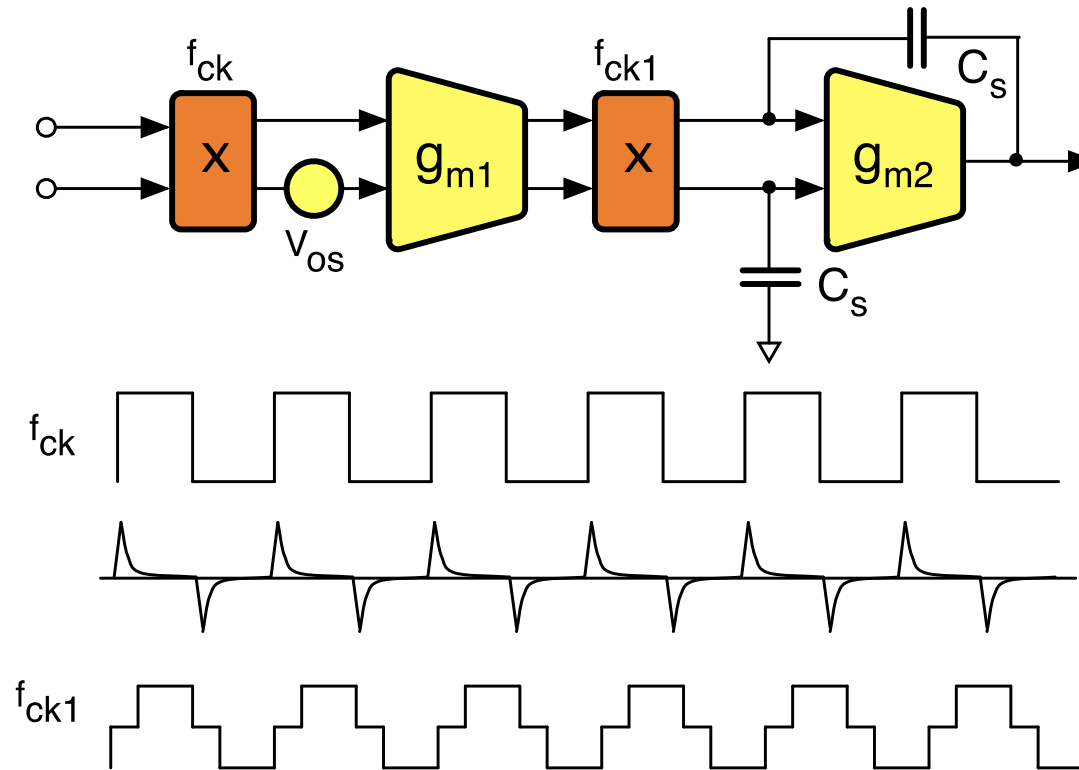
Nested Chopper

Bakker, A.; Thiele, K.; Huijsing, J.H.; "A CMOS nested-chopper instrumentation amplifier with 100-nV offset "
IEEE JSSC, pp.1877-1883, 2000

	Value	Unit
Supply Voltage	5	Volt
Supply Current	200	μA
High chopping	2	kHz
Low Chopping	16	Hz
Offset	100	nV
Offset TC (20-50 °C	3	nV/°C
Input referred Noise	27	nV/sqrt(Hz)
CMRR	140	dB

4.3 Offset compensation

Guard Interval Time



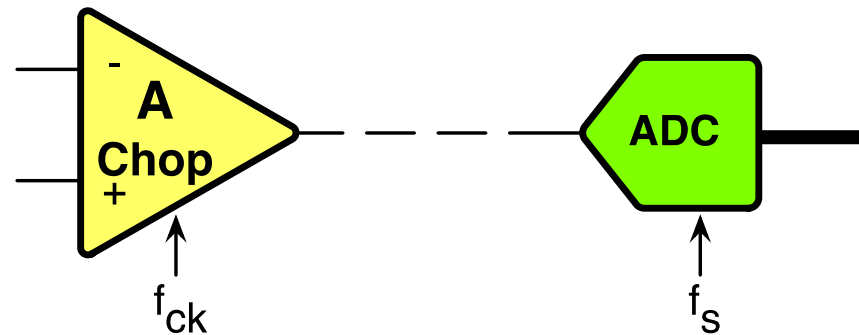
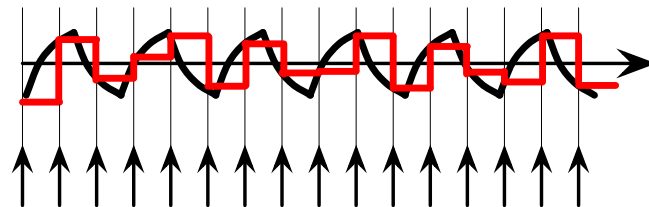
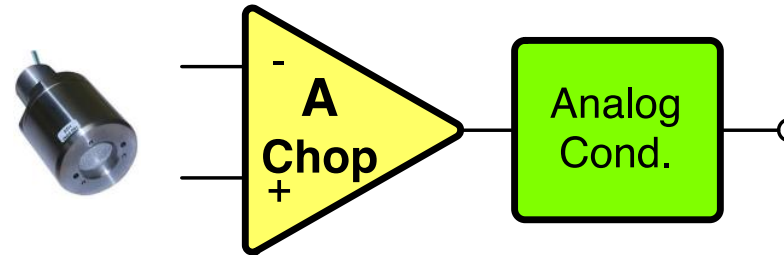
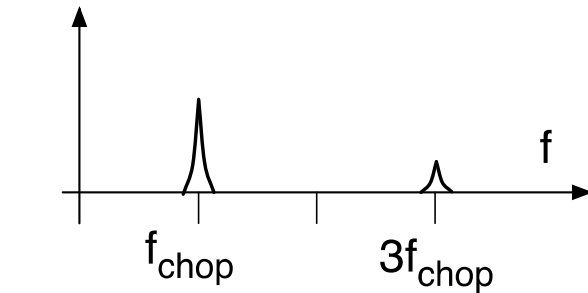
- Wait the time required to vanish the glitch

Menolfi, C.; Huang, Q.; "A 200 nV offset 6.5 nV/√Hz noise PSD 5.6 kHz chopper instrumentation amplifier in 1 μm digital CMOS" *IEEE ISSCC*, pp.362-363, 465, 2001

4.3 Offset compensation

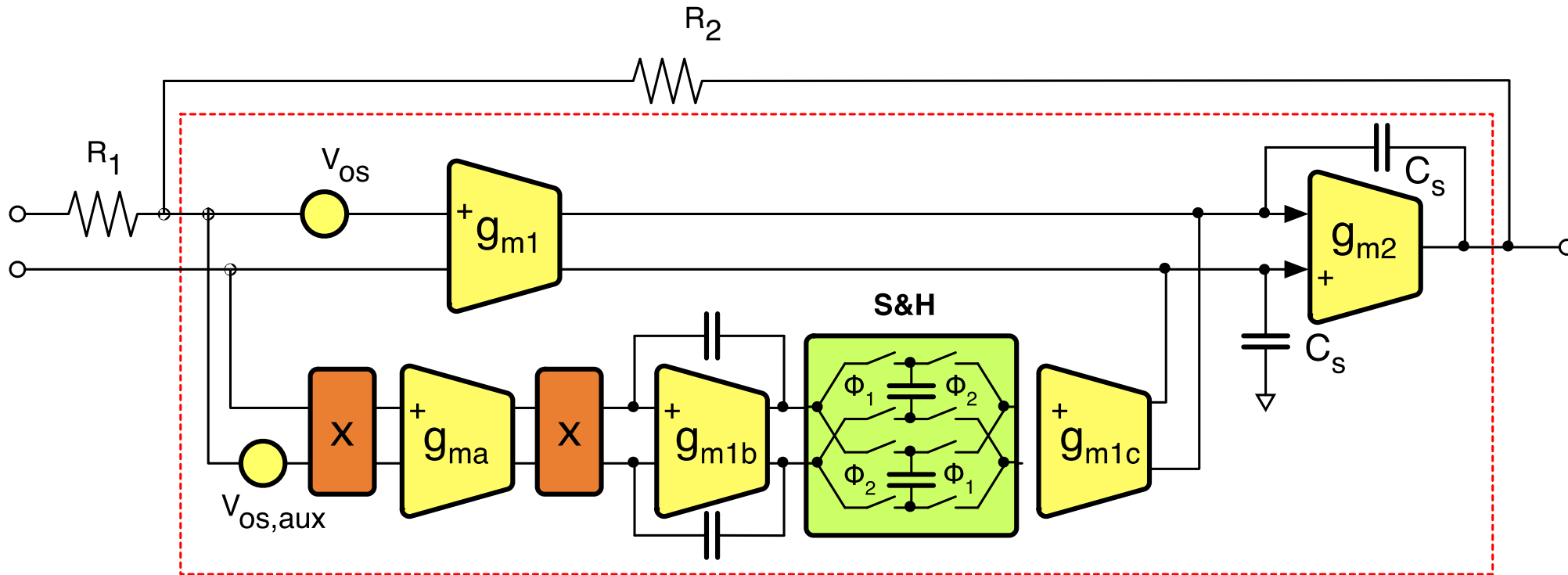
ANOTHER LIMIT: Ripple

Ripple → voltage or current spur occurring at the chopper frequency caused by switching between offset levels

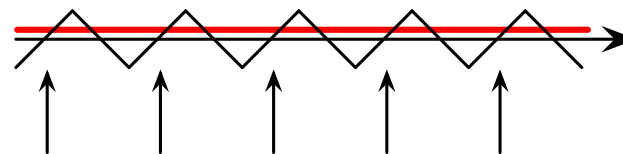


4.3 Offset compensation

Solution 2: Use of S&H as a notch filter



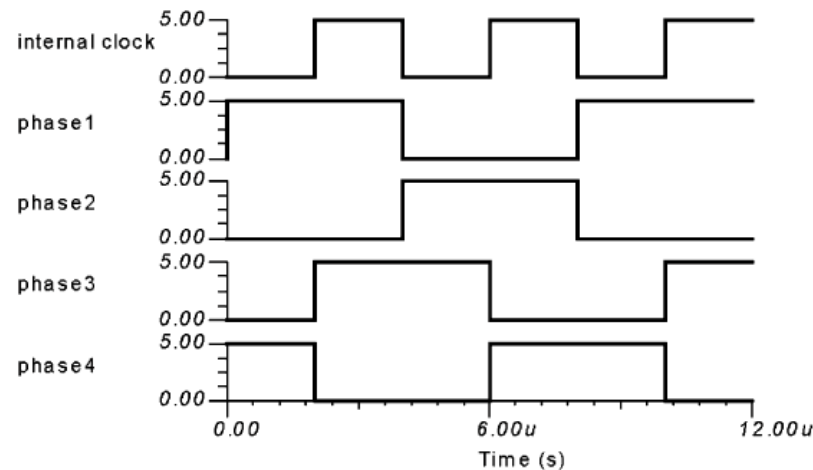
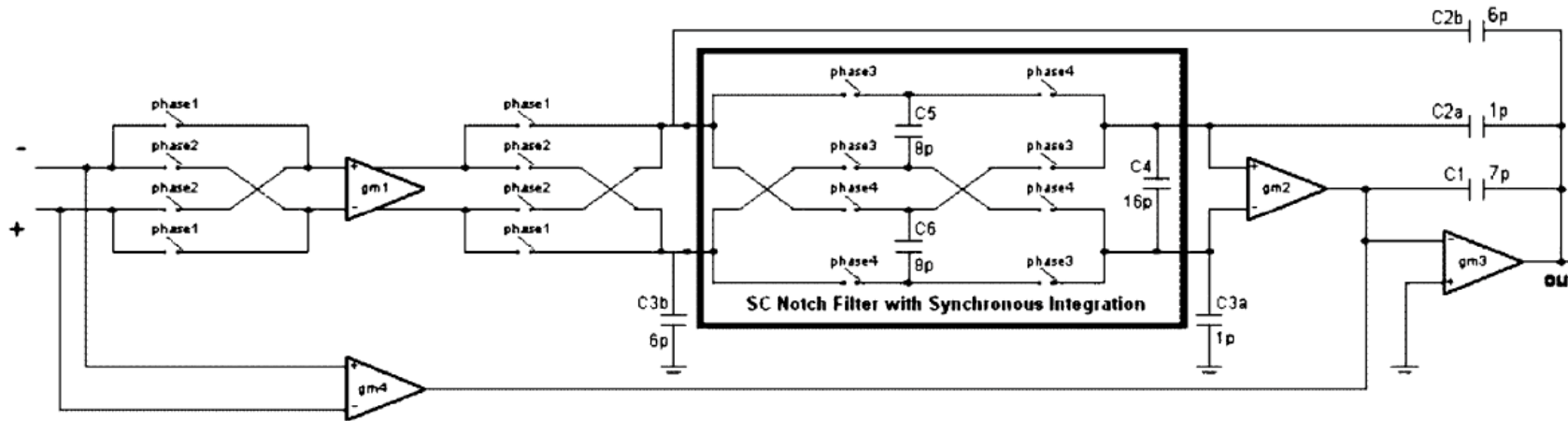
- Use as sampling times the zero crossing of the ripple



Witte, J.F.; Makinwa, K.A.A.;
Huijsing, J.H.; "A CMOS Chopper
Offset-Stabilized Opamp" *IEEE
JSSCC*, pp. 1529 -1535, 2007

4.3 Offset compensation

Solution 2: Use of a notch filter

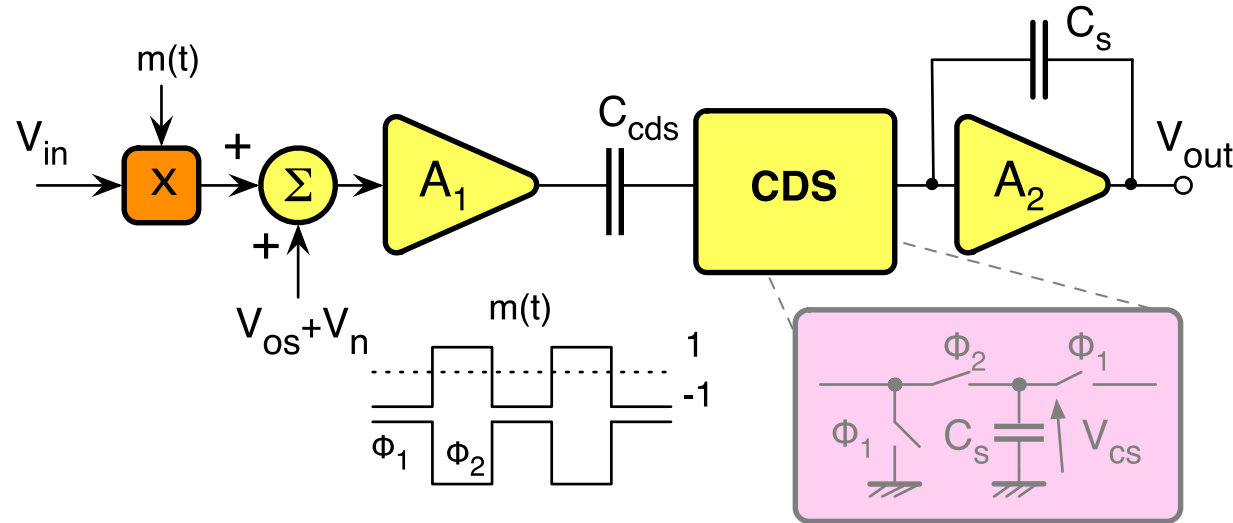


Burt, R.; Zhang, J.; "A Micropower Chopper-Stabilized Operational Amplifier Using a SC Notch Filter With Synchronous Integration Inside the Continuous-Time Signal Path", *IEEE JSSCC*, pp.2729-2736, 2006

- Integrate the offset generated current using the storing capacitor

4.3 Offset compensation

Solution 3: Use of CDS

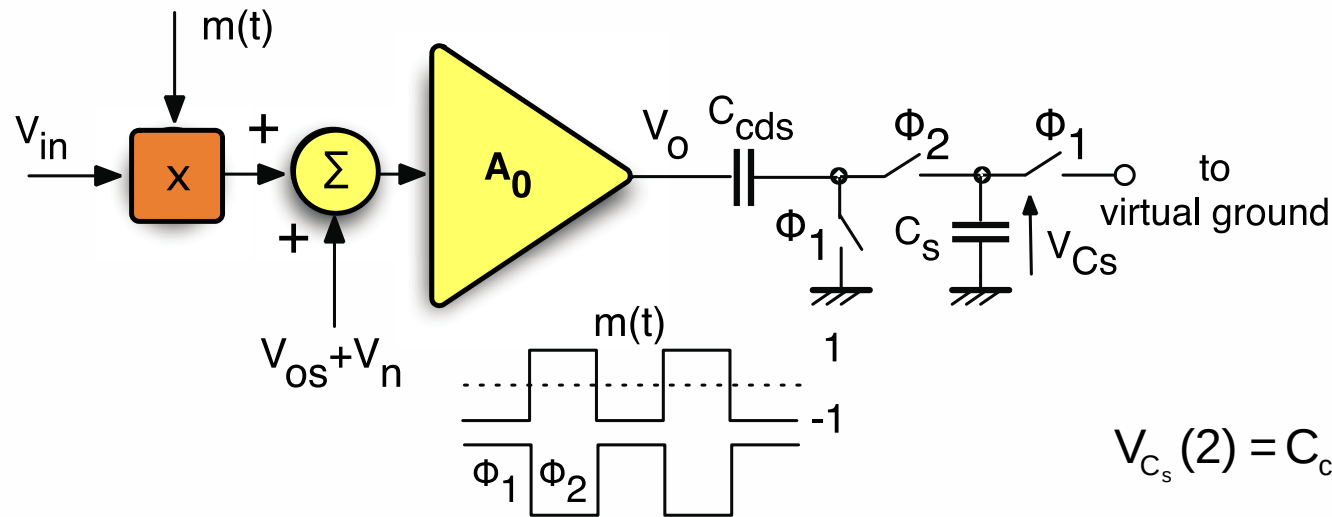


If offset and 1/f noise do not saturate the gain stage, their contribution is removed by AC coupling while the signal is detected by the correlated-double sampling scheme

Result: Ripple-free operation

Belloni, M.; Bonizzoni, E.; Fornasari, A.; Maloberti, F.; "A Micropower Chopper-CDS Operational Amplifier", *IEEE JSSC*, pp. 2521-2529, 2010

4.3 Offset compensation



$$V_{C_s}(2) = C_{cds} \frac{-V_o(1) + V_o(2)}{C_{cds} + C_s}$$

$$V_o(1) = A_0[-V_{in}(1) + V_{os} + V_n(1)]$$

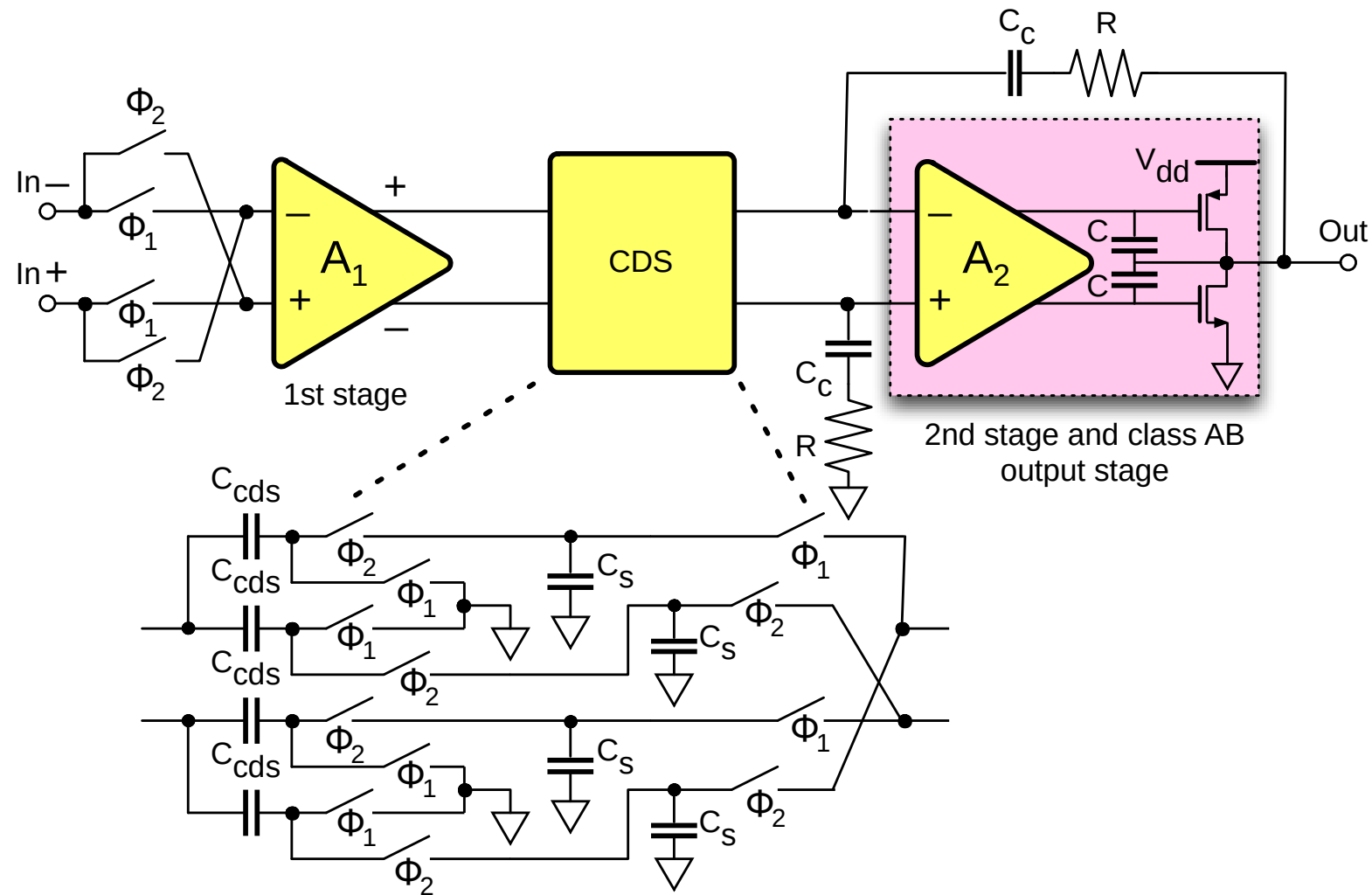
$$V_o(2) = A_0[V_{in}(2) + V_{os} + V_n(2)]$$

$$Q_{cds}(1) = -V_o(1)C_{cds} \quad \text{and} \quad Q_{C_s}(1) = 0$$

$$-V_o(1) + V_o(2) = A_0[V_{in}(1) + V_{in}(2) + \cancel{V_{os}} - \cancel{V_{os}} - V_n(1) + V_n(2)]$$

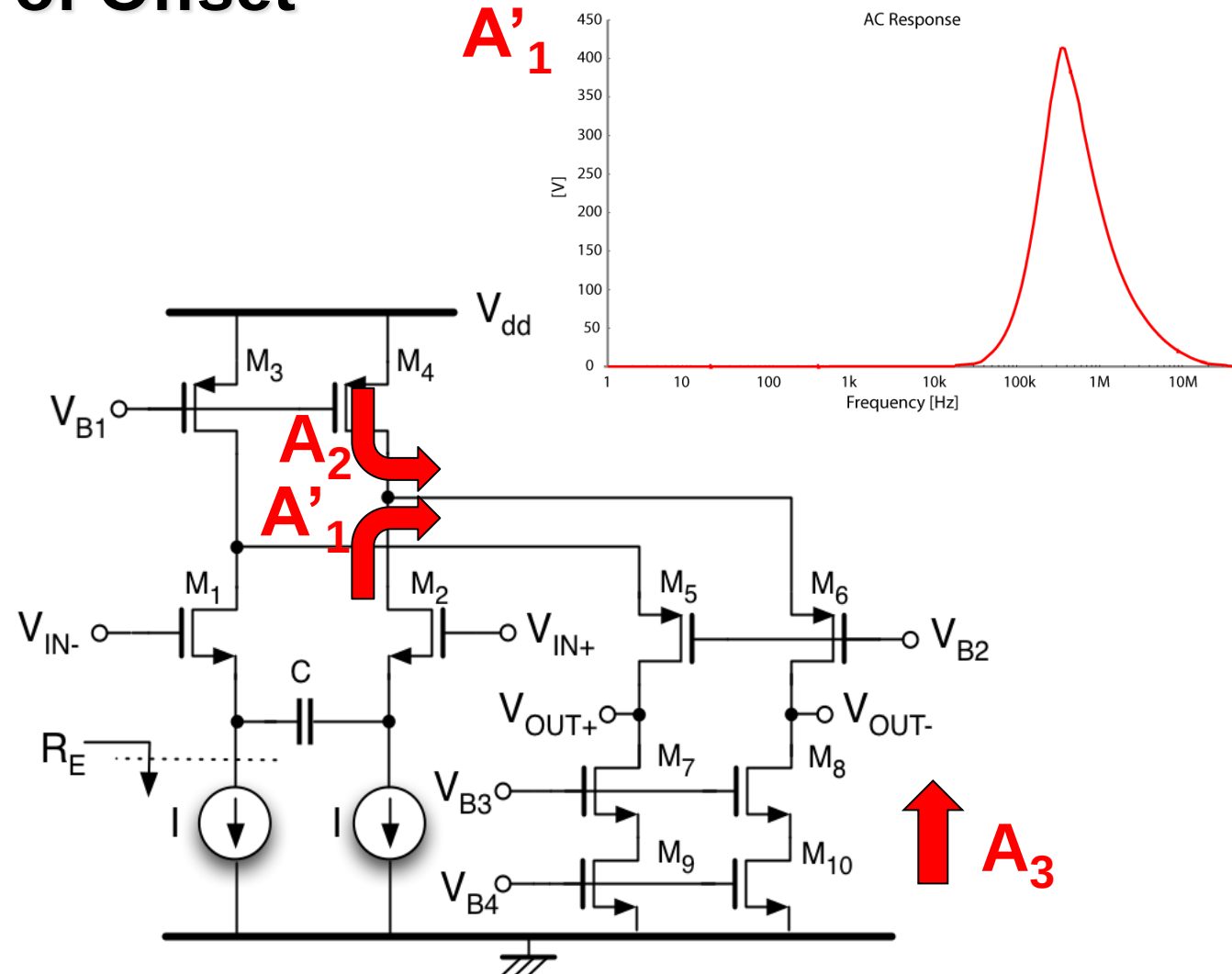
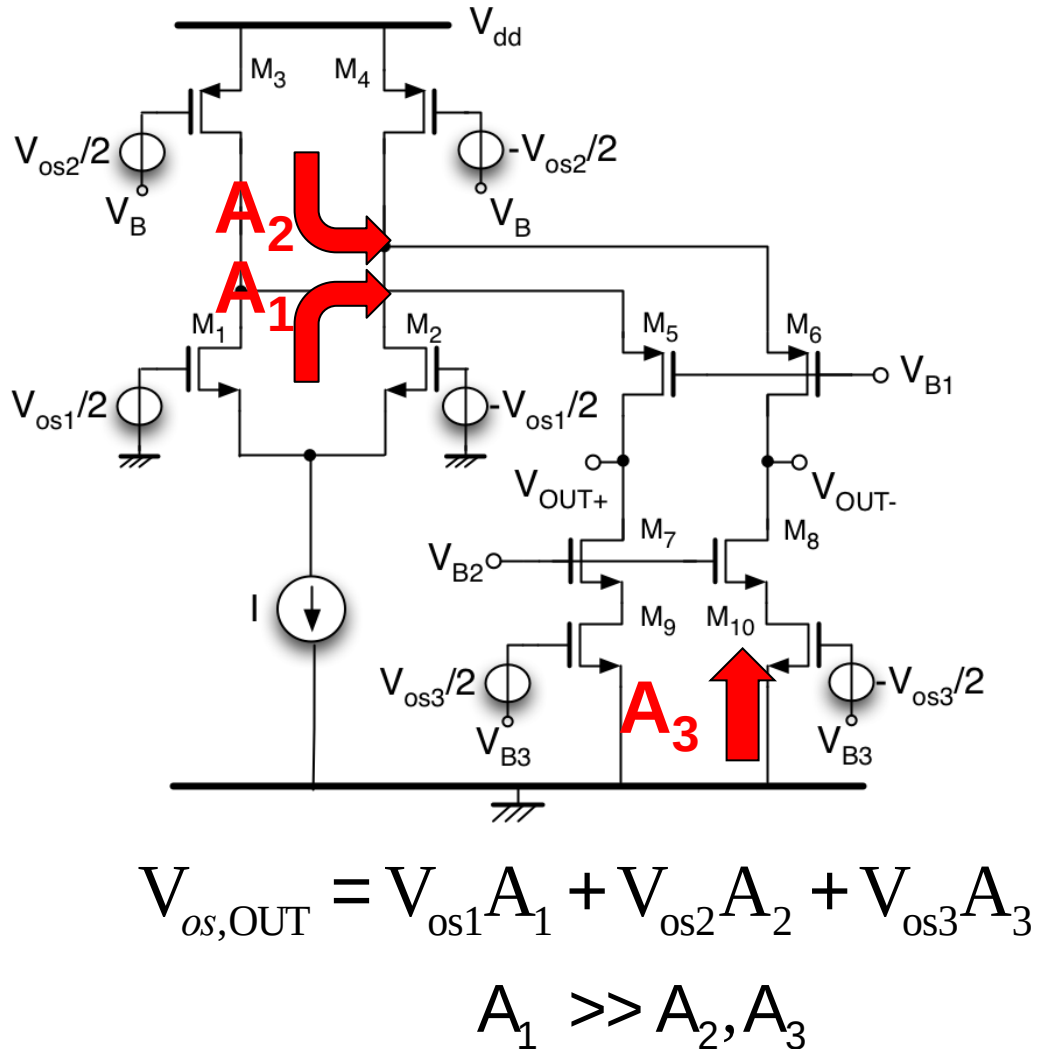
$$V_{C_s}(2) = \frac{A_0 C_{cds} [V_{in}(1) + V_{in}(2) - V_n(1) + V_n(2)]}{C_{cds} + C_s}$$

4.3 Offset compensation



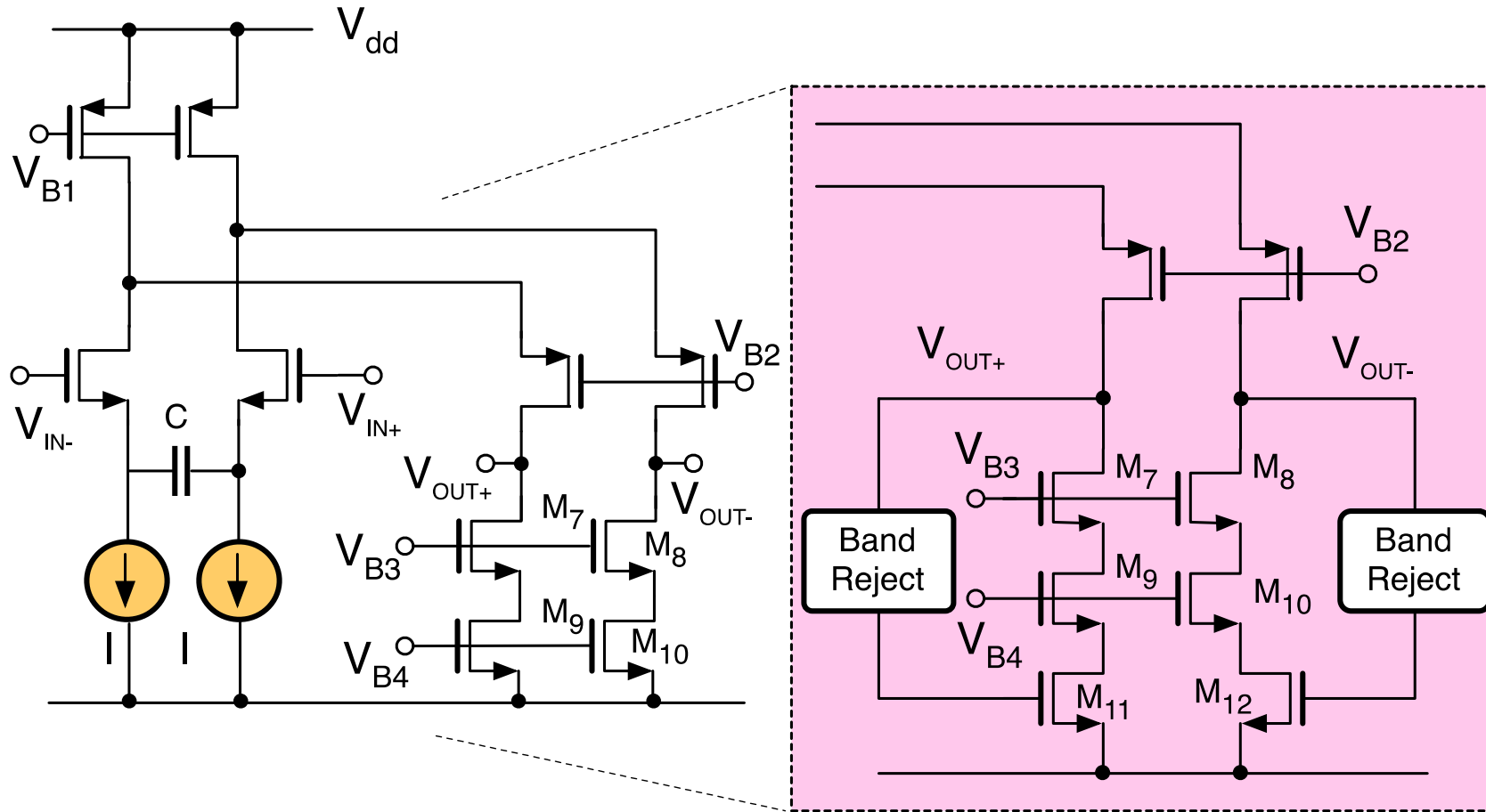
4.3 Offset compensation

Sources of Offset

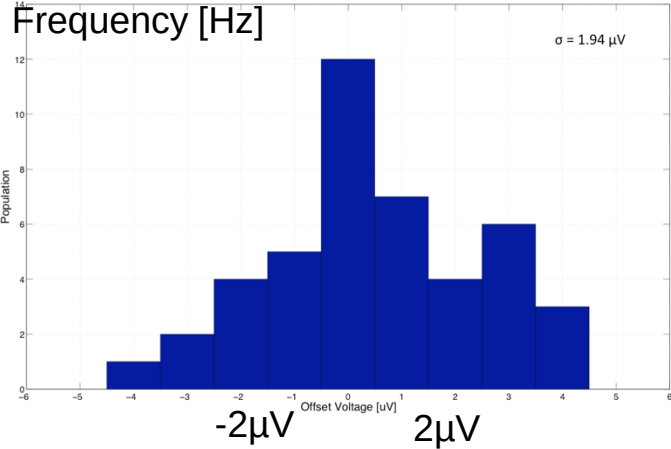
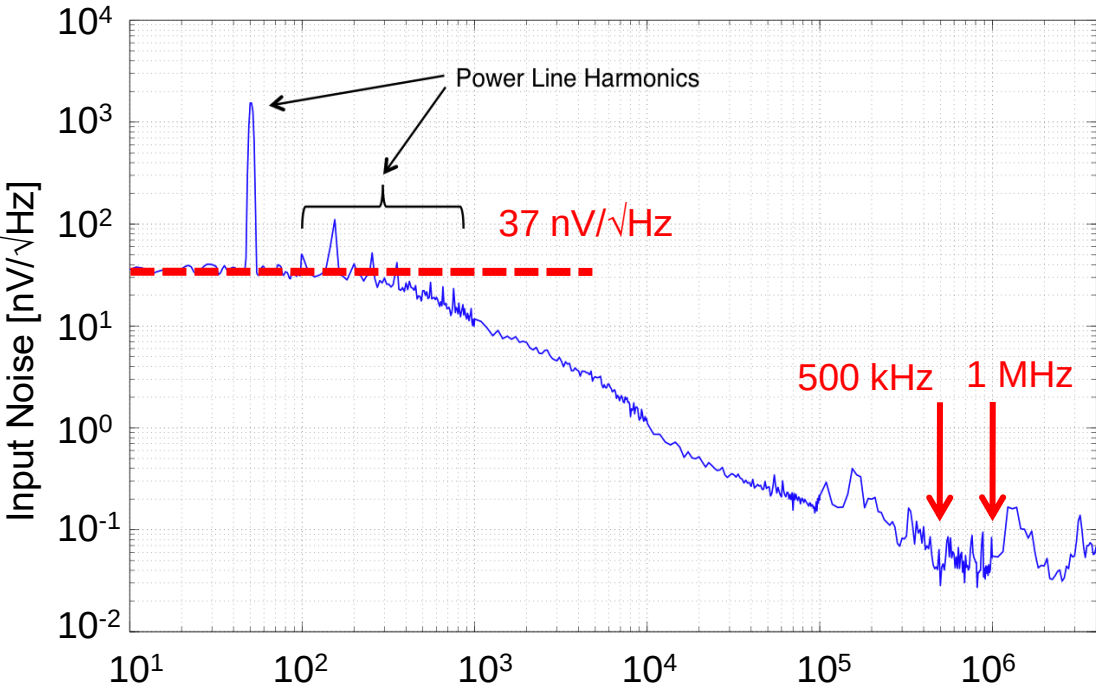


4.3 Offset compensation

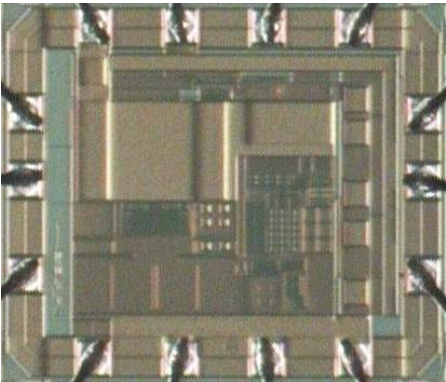
Diminish the Other Gains



4.3 Offset compensation



Supply Voltage	1.8→5V
Chopping Frequency	500kHz
Input Noise Density at DC	37nV/√Hz
Offset Voltage Standard Deviation	1.94μV
Analog Supply Current	12.8μA
Digital Supply Current	1.6μA
Common Mode Input Range	0→5V
GBW (extrapolated)	260kHz
Offset Temperature Dependence	<0.03μV/°C
Process	Mixed 0.18-0.5μm CMOS
Chip Area (Including Pads)	1.21mm x 0.95mm
Noise Efficiency Factor	5.5



5. Analog to Digital Conversion

Content

- 5.1 Analog to Digital Converters
- 5.2 SAR Converters
- 5.3 Sigma Delta and Incremental Converters

5.1 Analog to Digital Converters

Analog-to-digital Converters for Energy Harvesting Systems

Key elements for a low-power operation are :

- ❖ Suited ADC conversion principle.
- ❖ Low voltage operation of the ADC.
- ❖ Capability of the ADC to quickly wake-up, convert and stand-by again.
- ❖ Low leakage of the ADC when in standby.

The lowest power conversion principles are usually:

- ❖ 8 to 10-bit range : capacitive SAR ADC
- ❖ 10 to 12-bit range : Hybrid SAR, oversampled or incremental ADC
- ❖ 12 to 16-bit range : oversampled/incremental or hybrid ADC

5.1 Analog to Digital Converters

Key ADC parameters

Nominal resolution [bits] : hypothetical maximal resolution of the conversion.

Sampling rate [Sample/second] : output data rate.

Input bandwidth [Hz] : bandwidth of sampling stage.

Signal to Noise Ratio (SNR) [dB] : obtained from output FFT when a maximal amplitude signal is sampled. Ratio of digitized signal power over noise power.

Signal to Noise and Distorsion Ratio (SNDR or SINAD) [dB] : same as SNR but considering distorsion tones (harmonics) as noise.

Effective Number of bit (ENB) [bits] : SNDR expressed in [bits]. $ENB = (SNDR [dB] - 1.76) / 6.02$

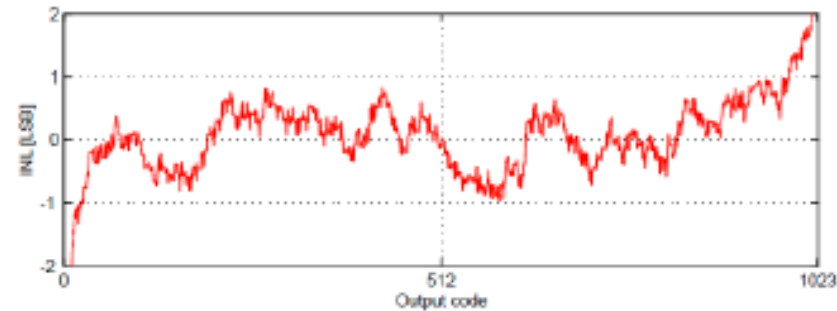
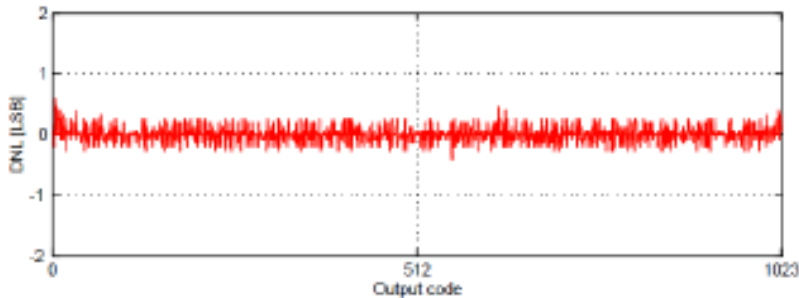
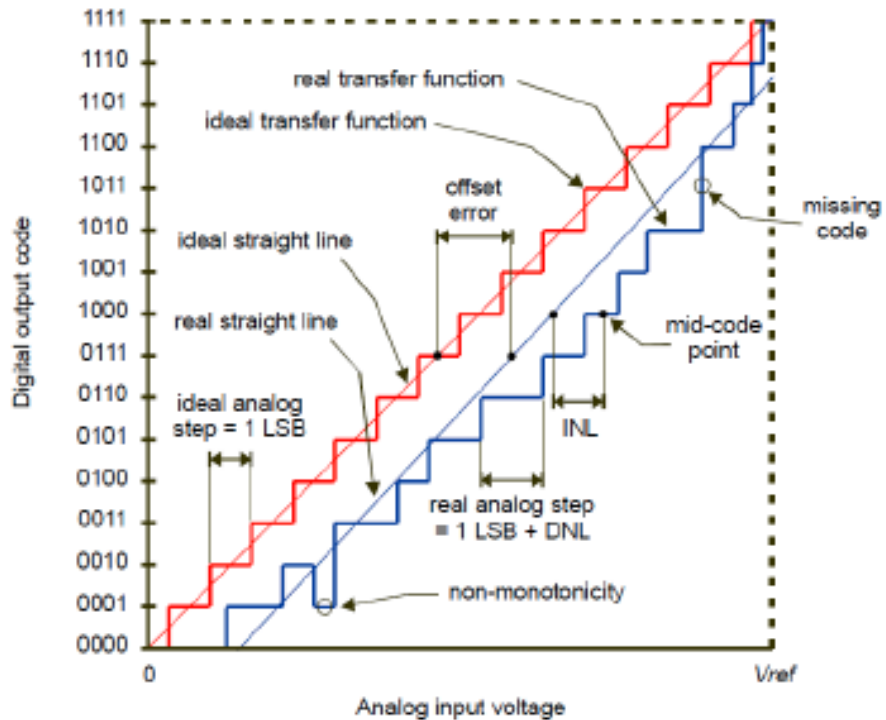
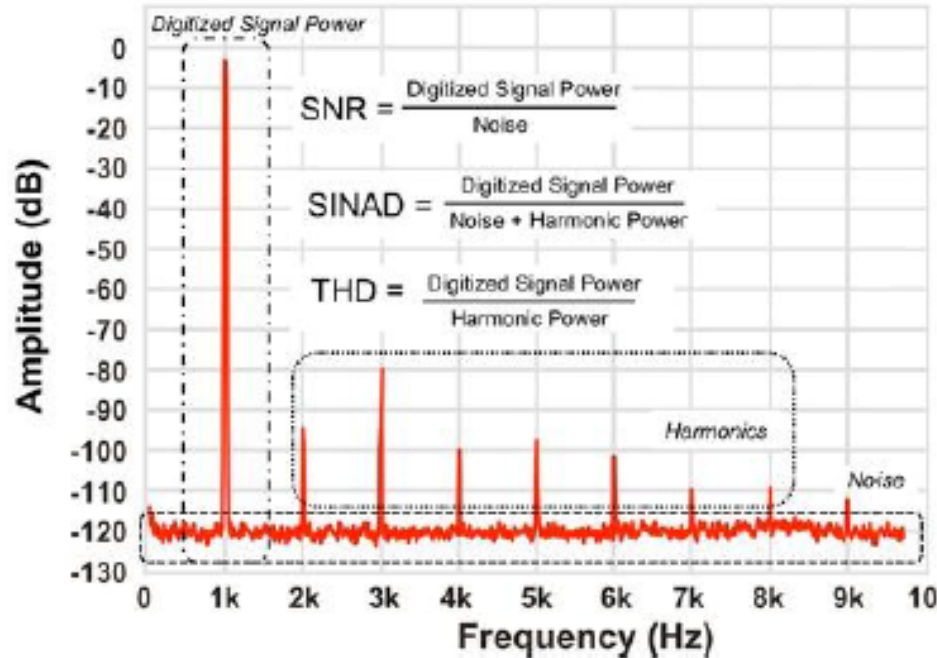
Spurious-free Dynamic Range (SFDR) [dB] : power ratio between highest fundamental tone and highest harmonics.

Differential Non-Linearity (DNL) [LSB] : input linearity error for each digital code

Integral Non-Linearity (INL) [LSB] : linearity error separating ideal transfer curve from real one. This is also the integration of the DNL errors.

5.1 Analog to Digital Converters

Key ADC parameters



5.1 Analog to Digital Converters

Figure of Merit

- There are (at least) two widely used ADC figures of merit (FOM) used in literature
- **Walden FOM**
 - Energy increases 2x per bit (ENOB)
 - Empirical

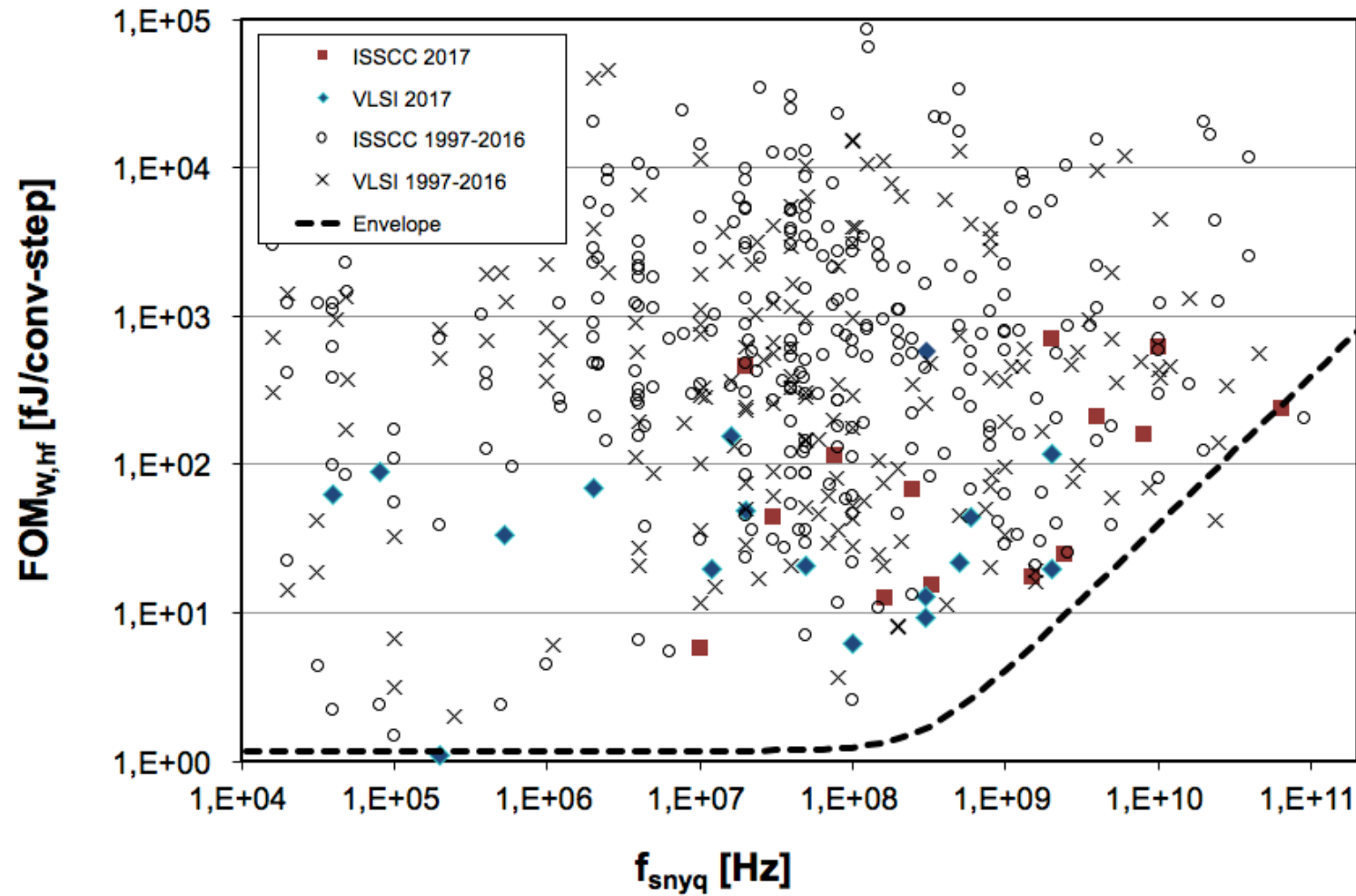
$$\text{FOM} = \frac{\text{Power}}{2^{\text{ENOB}} \cdot f_{\text{snyq}}}$$

- **Schreier FOM**
 - Energy increases 4x per bit (DR)
 - Thermal
 - Ignores distortion

$$\text{FOM} = \text{DR}(\text{dB}) + 10 \log \left(\frac{\text{BW}}{P} \right)$$

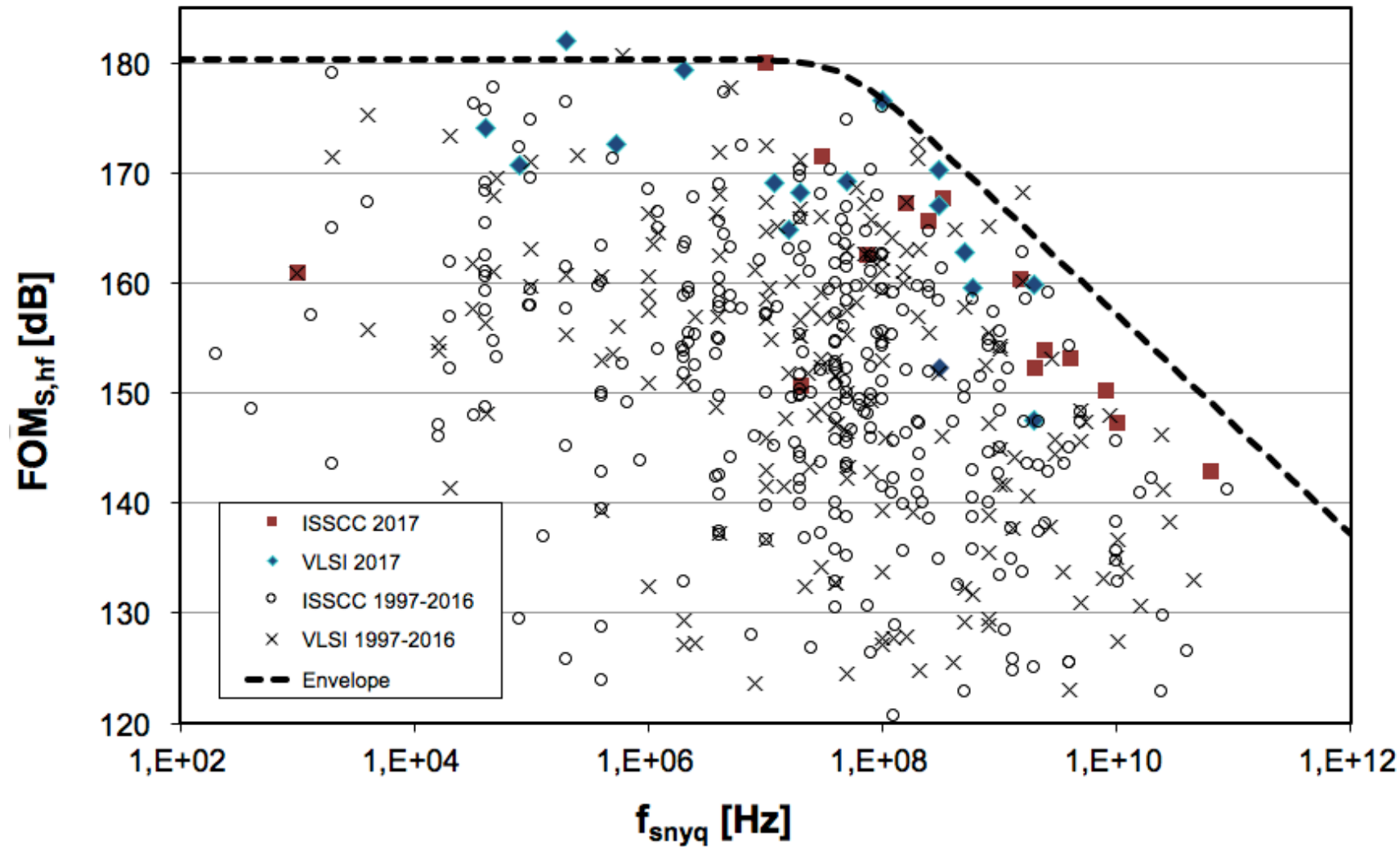
R. H. Walden, "Analog-to-digital converter survey and analysis," *IEEE Journal on Selected Areas in Communications*, April 1999

5.1 Analog to Digital Converters



<https://web.stanford.edu/~murmman/adcsurvey.html>

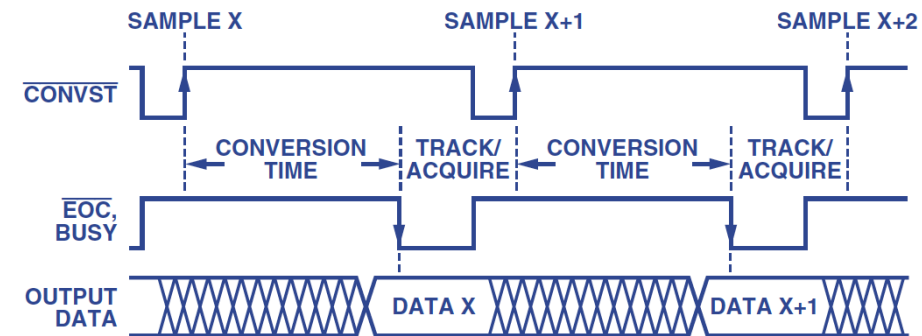
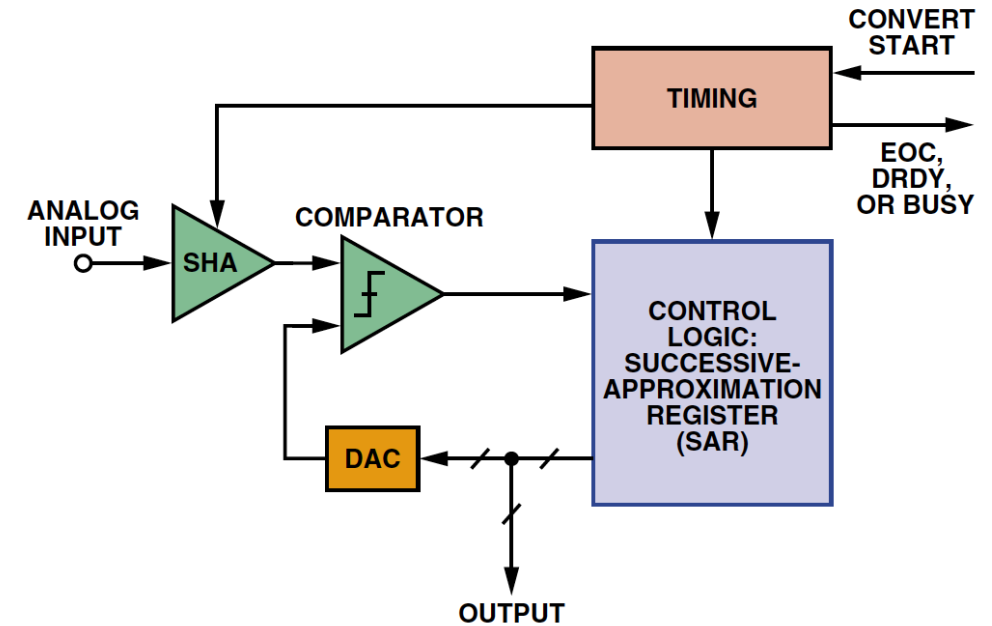
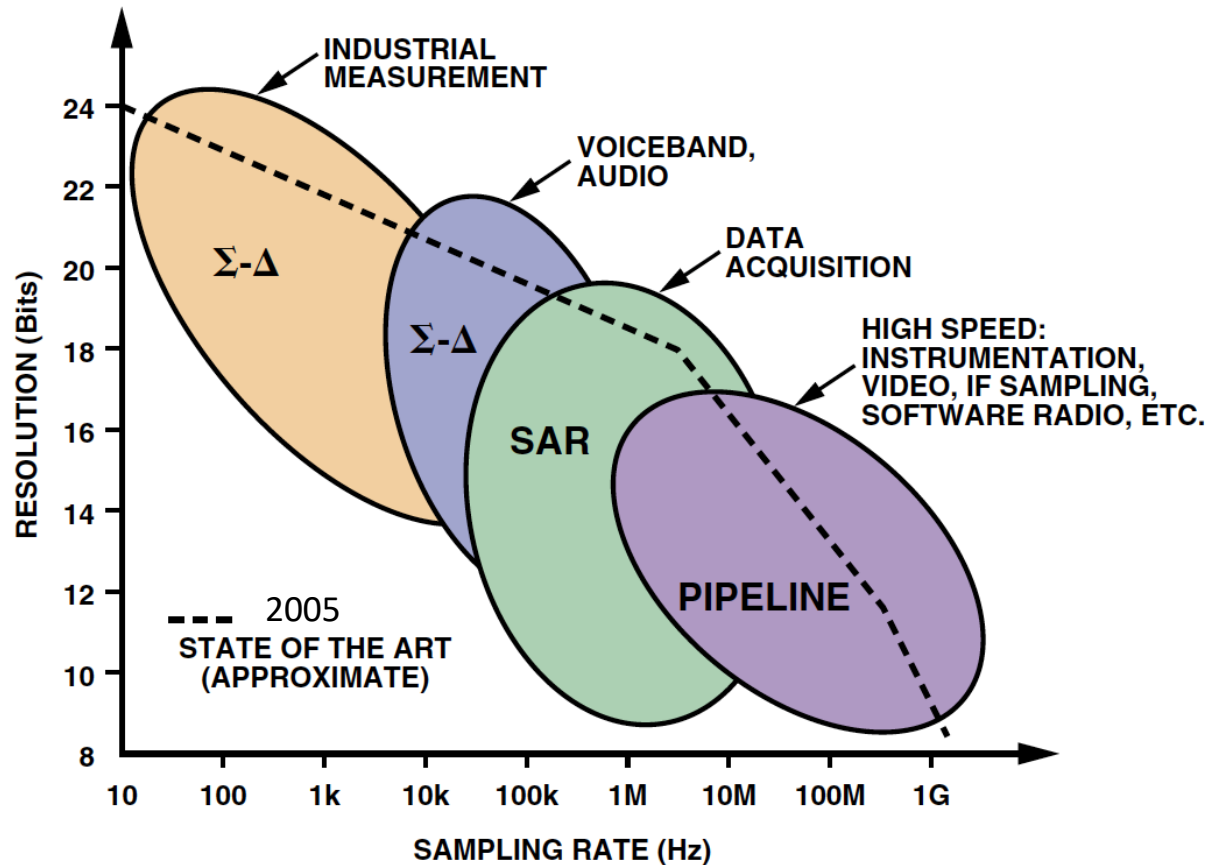
5.1 Analog to Digital Converters



<https://web.stanford.edu/~murmman/adcsurvey.html>

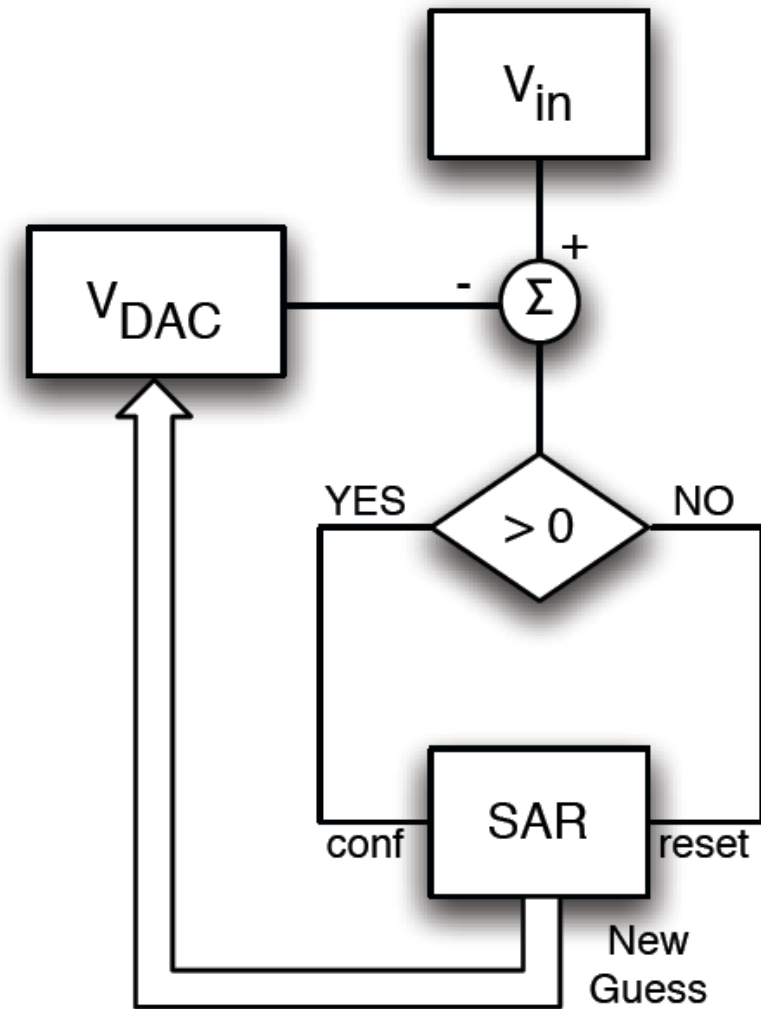
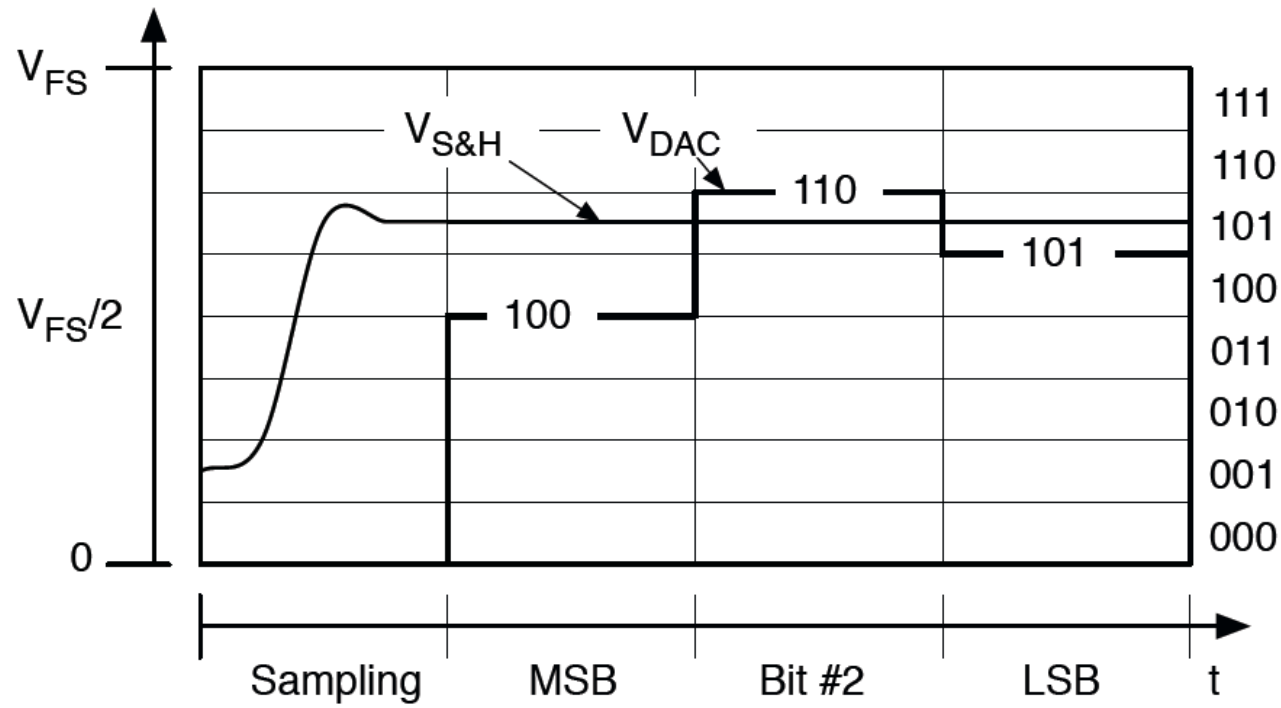
5.1 Analog to Digital Converters

- CHOICE OF ARCHITECTURE



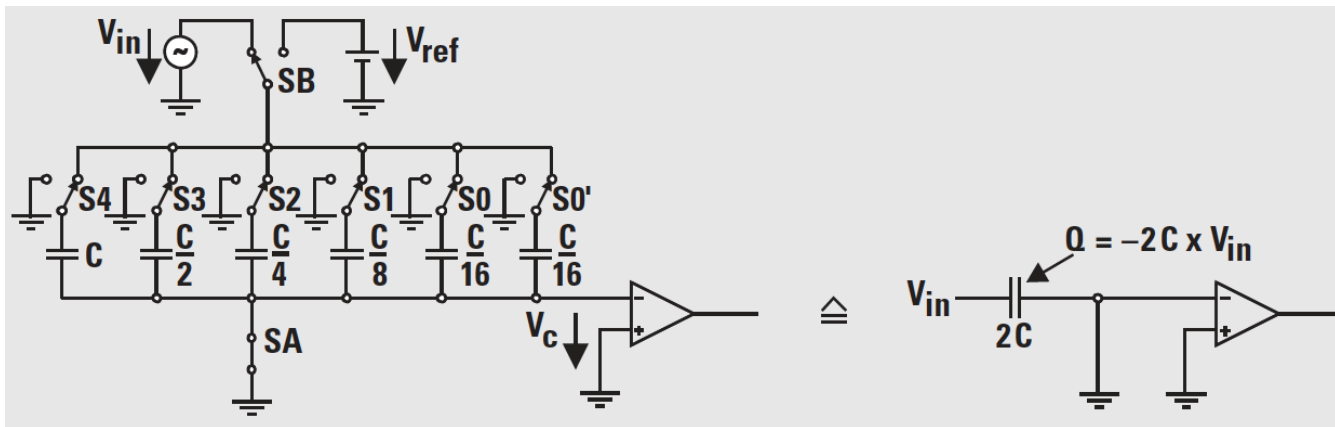
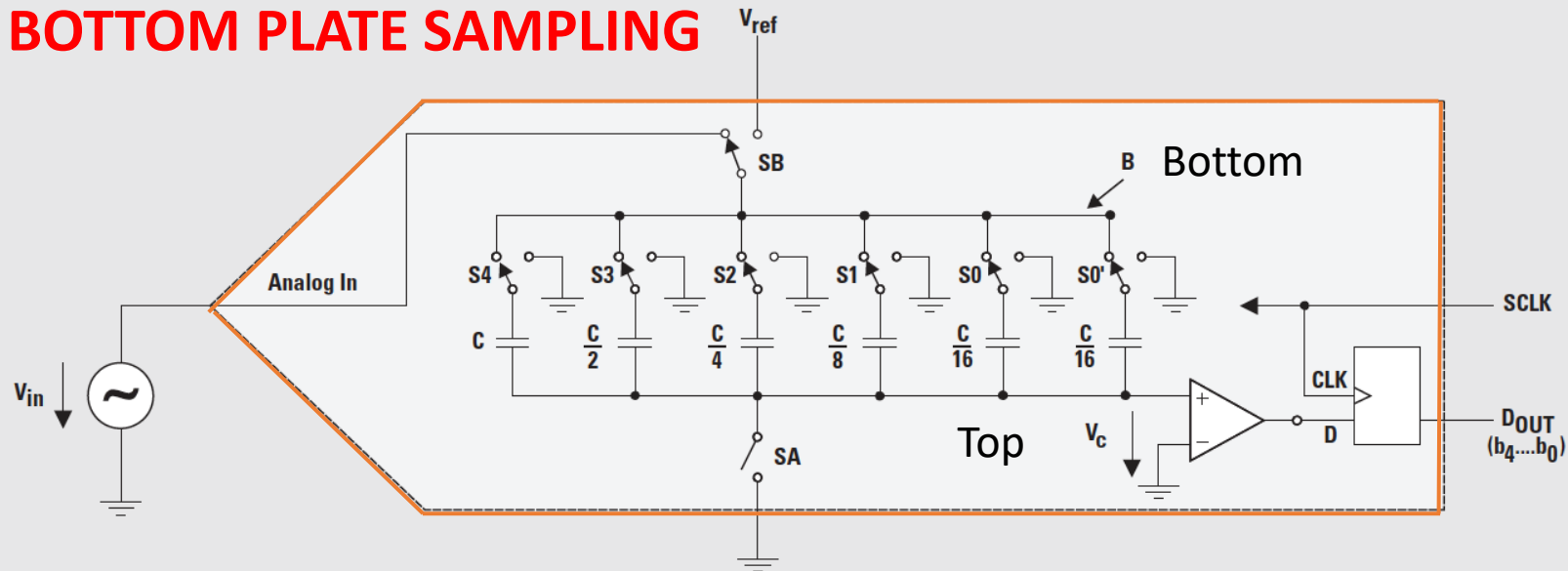
5.2 SAR Converters

- The successive approximation converter obtains the A/D conversion in successive steps; typically one bit per clock period



5.2 SAR Converters

BOTTOM PLATE SAMPLING



SAMPLING

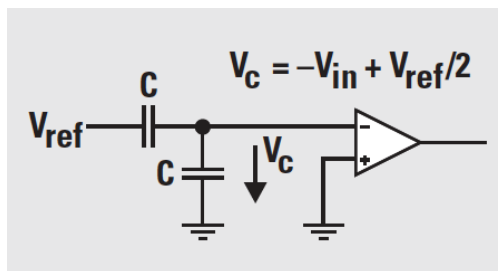
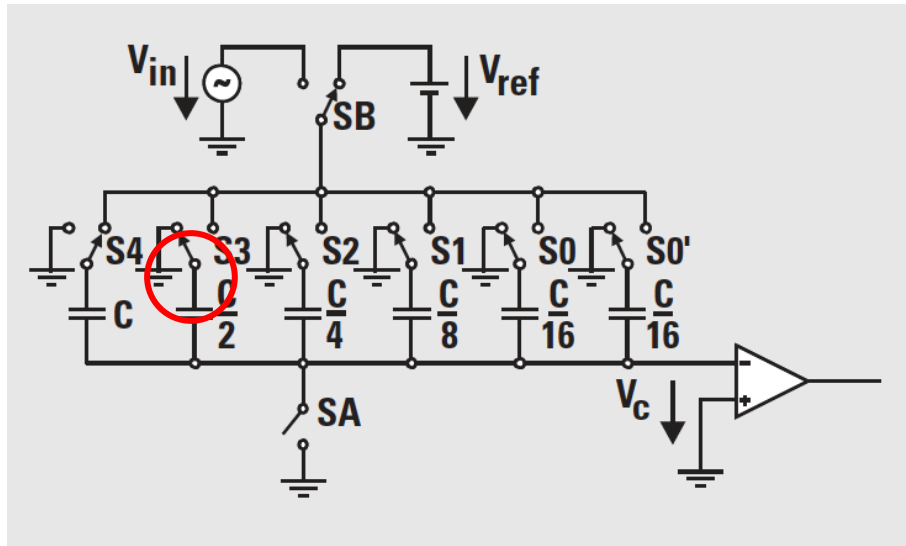
Input load $2C$

Same Common-mode of comparator at the beginning and the end

5.2 SAR Converters

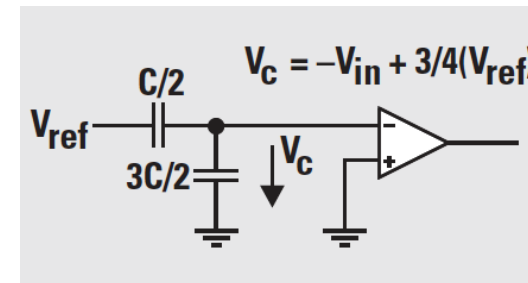
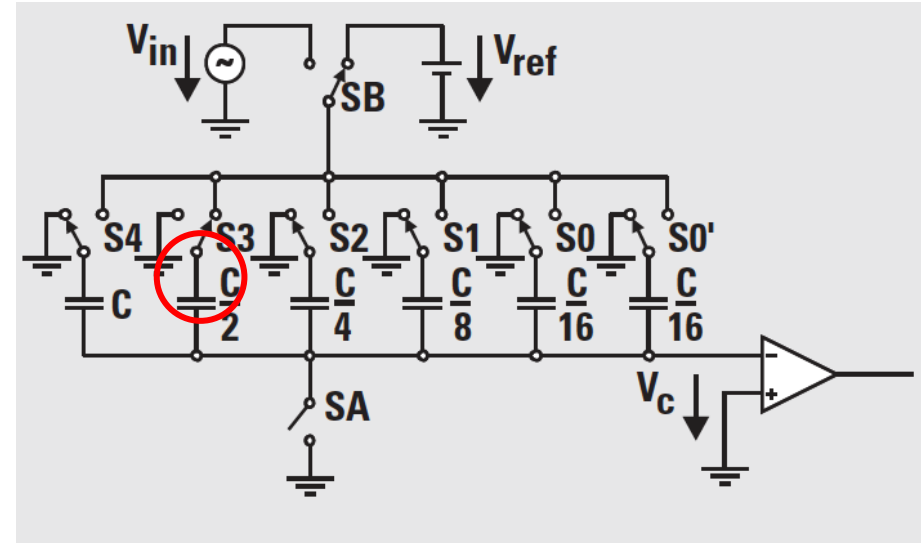
CHARGE REDISTRIBUTION

MSB



$$Q = -CV_{in} \rightarrow Q = C(-V_{in} + V_{ref}/2)$$

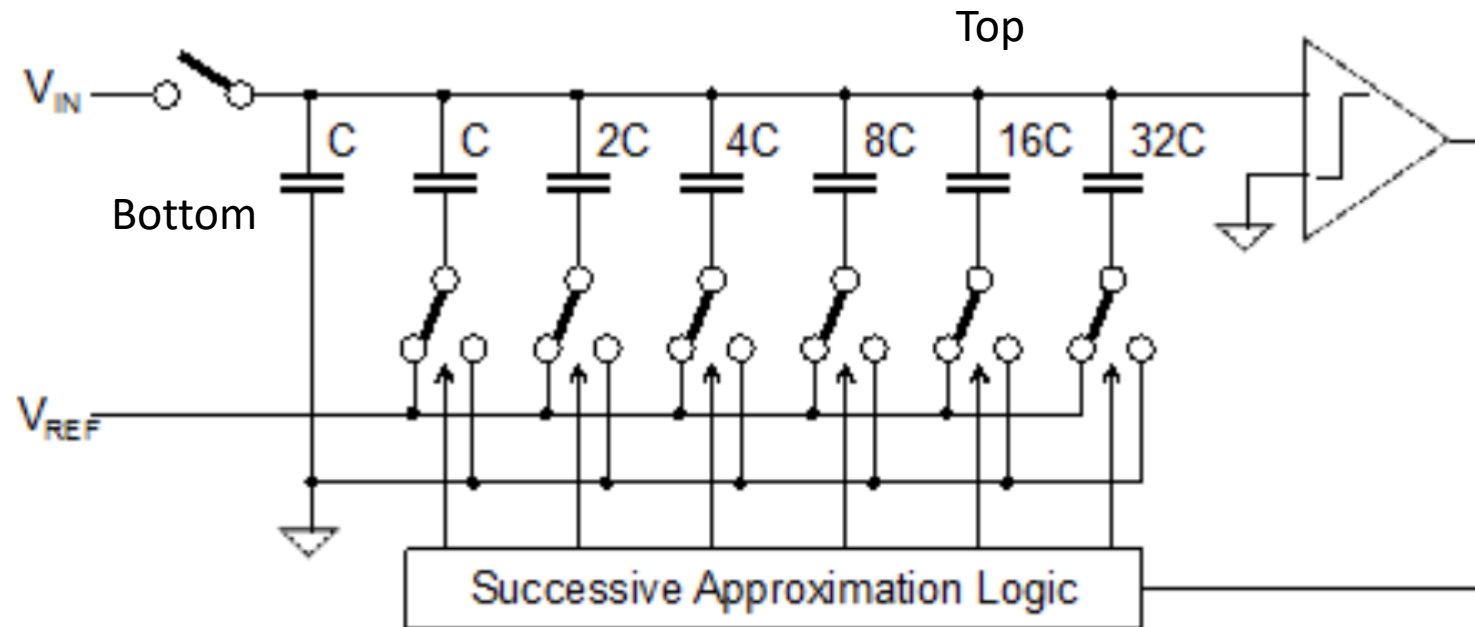
If MSB = 0 (MSB-1)



$$Q = 3/2C(-V_{in} + V_{ref}/2) \rightarrow Q = 3/2C(-V_{in} + 3V_{ref}/4)$$

5.2 SAR Converters

TOP PLATE SAMPLING

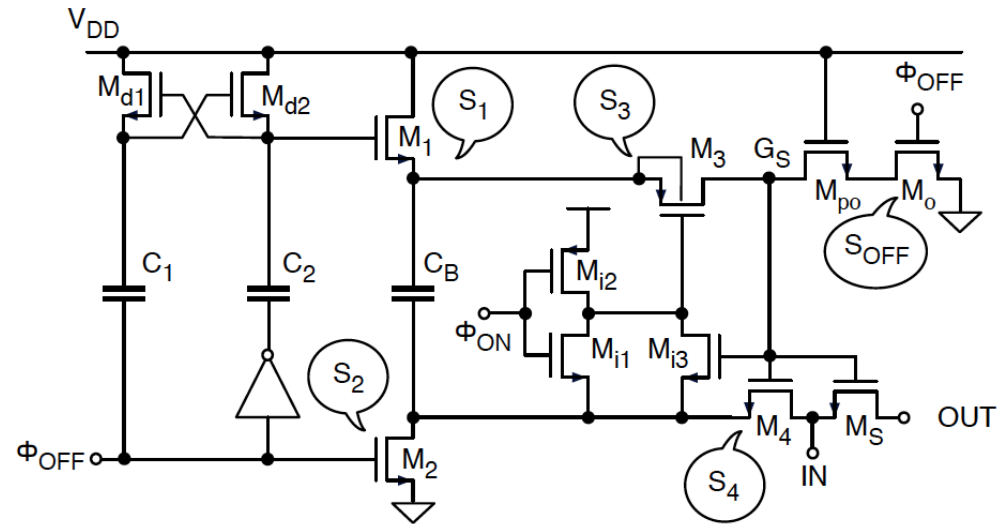
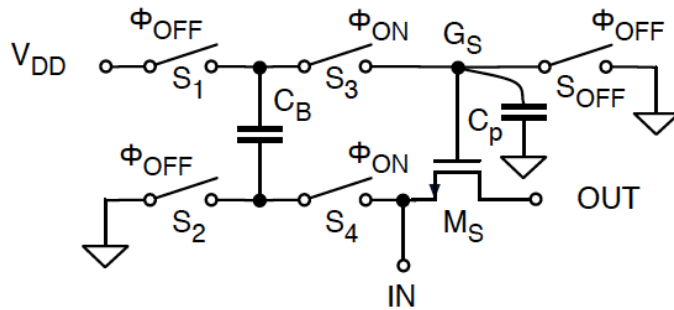


- The fully differential halves the number of unity capacitances
 - The input signal is already at the comparator input
- Error caused by clock feed-through
- Needs clock boost

5.2 SAR Converters

HOW TO FIRMLY CLOSE A SWITCH

- Use of clock boost



- The idea is to use a V_{GS} constant independent on the input voltage
- The boosting capacitor ideally establishes $V_{GS}=V_{DD}$

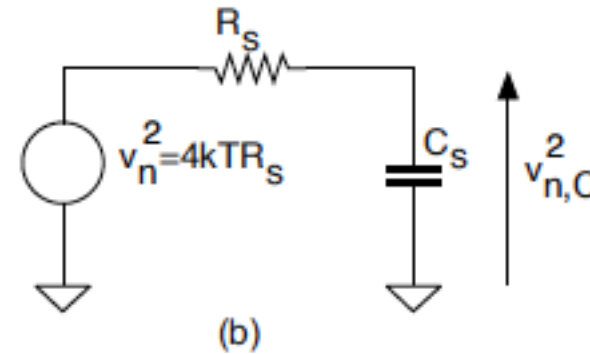
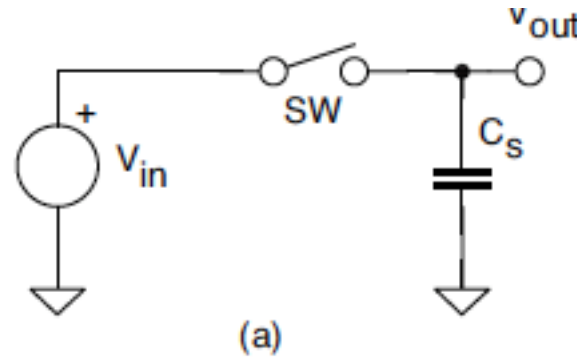
$$V_G = (V_{DD} + V_{in}) \frac{C_B}{C_B + C_p}$$

- The parasitic capacitance causes an input voltage dependence of the channel charge

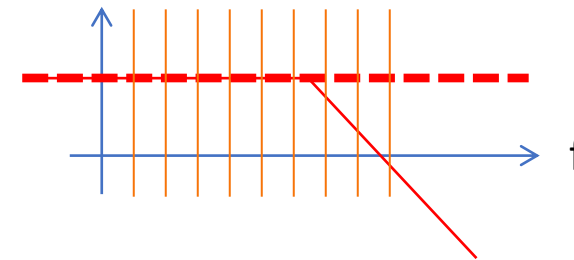
5.2 SAR Converters

SAMPLING CAPACITANCE VALUE (KT/C)

- Any sampling operation gives rise to noise. The model used is



$$v_{n,C_s}^2(\omega) = \frac{4kTR_s}{1 + (\omega R_s C_s)^2}$$



$$P_{n,C_s} = \int_0^\infty v_{n,out}(f) df = 4kTR_s \int_0^\infty \frac{df}{1 + (2\pi f R_s C_s)^2} = \frac{kT}{C_s}$$

5.2 SAR Converters

SAMPLING CAPACITANCE VALUE (KT/C)

- The minimum capacitance used for sampling depends on V_{ref} and N_{bit}
- The condition kT/C noise equal to the quantization noise leads to

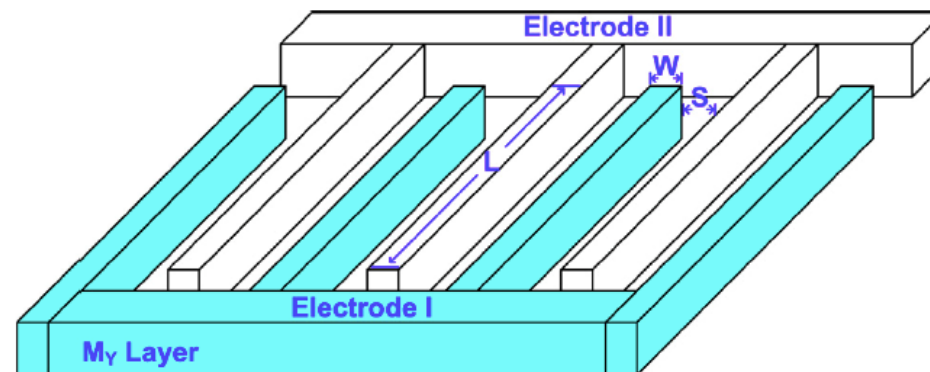
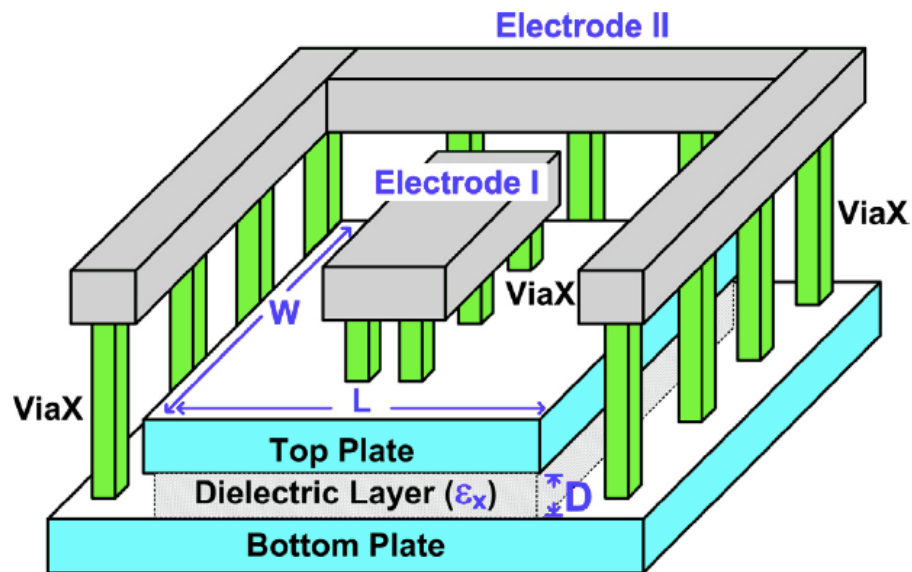
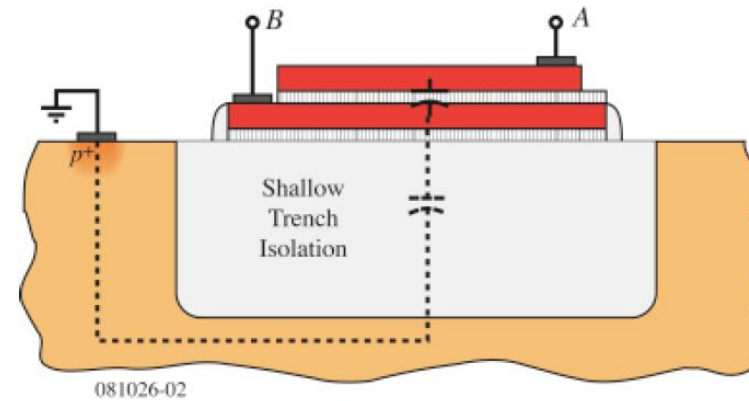
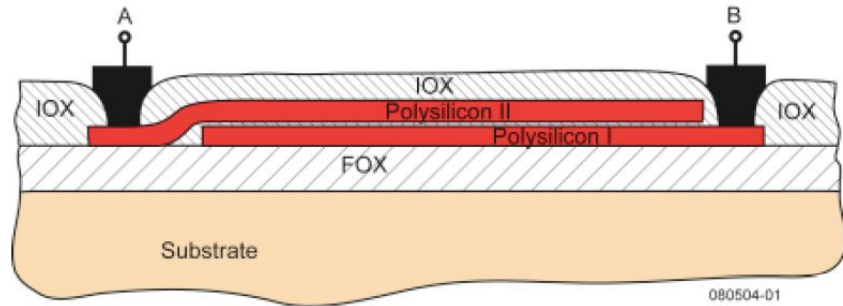
$$\frac{\Delta^2}{12} = kT/C$$

N-bit	$V_{\text{ref}}=1 \text{ V}$	$V_{\text{ref}}=1.2 \text{ V}$	$V_{\text{ref}}=1.5 \text{ V}$	$V_{\text{ref}}=1.8 \text{ V}$	$V_{\text{ref}}=2.5 \text{ V}$
6	2 fF	1.4 fF	0.9 fF	0.6 fF	0.3 fF
8	33 fF	22.7 fF	14.5 fF	10 fF	5.2 fF
10	52 fF	0.36 pF	0.23 pF	0.16 pF	83 fF
11	0.21 pF	1.45 pF	0.93 pF	0.64 pF	0.34 pF
12	0.84 pF	5.8 pF	3.7 pF	2.58 pF	1.34 pF
13	3.35 pF	2.3 pF	1.5 pF	10.3 pF	5.36 pF
14	13.4 pF	9.3 pF	5.95 pF	4.13 pF	2.14 pF

5.2 SAR Converters

CAPACITANCES

- There are many possible integrated structures for realizing capacitors



5.2 SAR Converters

SAMPLING CAPACITANCE VALUE (Mismatch)

- Mismatch is the process that causes time-independent random variations in physical quantities of identically designed devices
- The matching accuracy of integrated elements follows the Pelgrom equation

$$\sigma^2(\Delta P) = \frac{A_p^2}{WL} + S_P^2 D_x^2.$$

- Or more complicated relationships

$$3\sigma\left(\frac{\Delta C}{C}\right) = \sqrt{\frac{Ma}{W \cdot L} + \frac{Ml}{L^2} + \frac{Mw}{W^2}} \quad \%$$

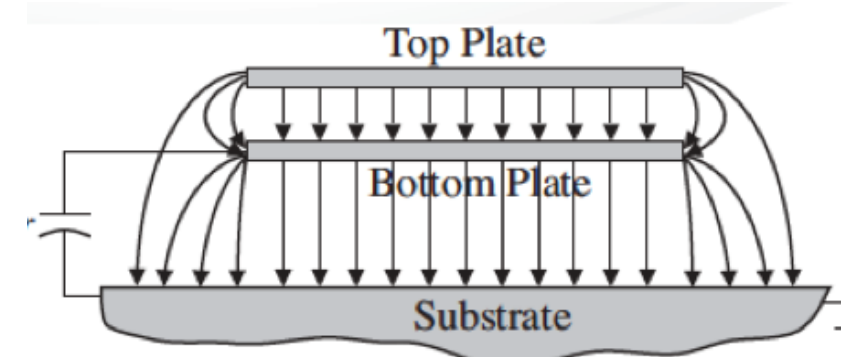
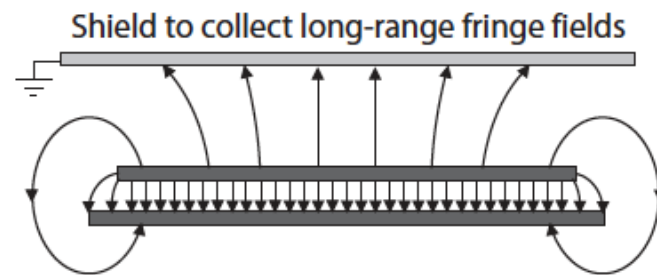
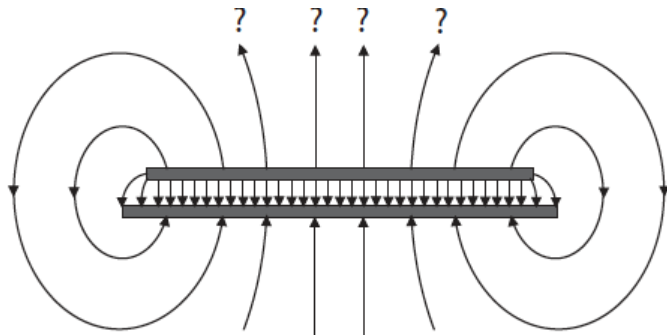
where

Ma	Ml
μm	μm
1.63	0.146

For a given technology

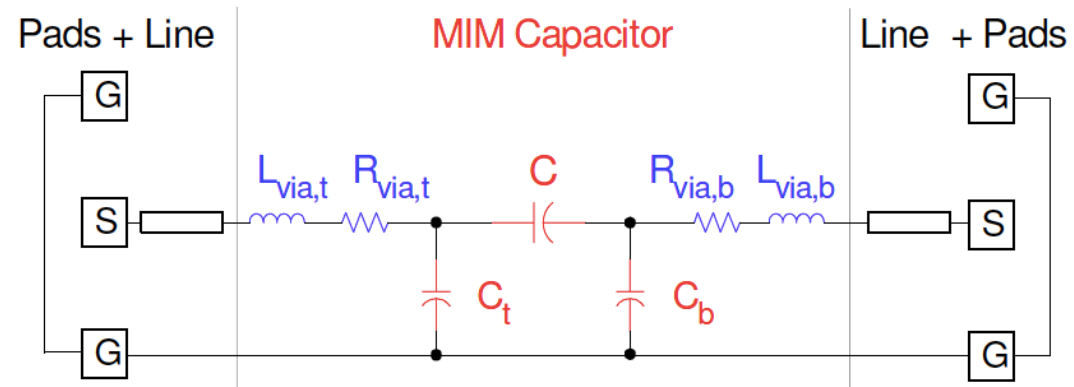
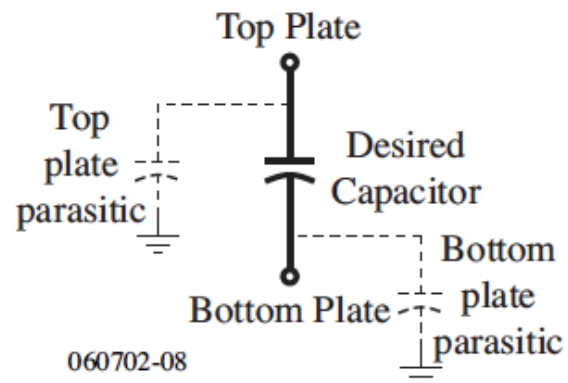
5.2 SAR Converters

Layout and matching



PARASITIC CAPACITANCES

- An integrated capacitor is not a “simple” capacitor



5.2 SAR Converters

SAR ARCHITECTURES

INCLUDING THE S&H

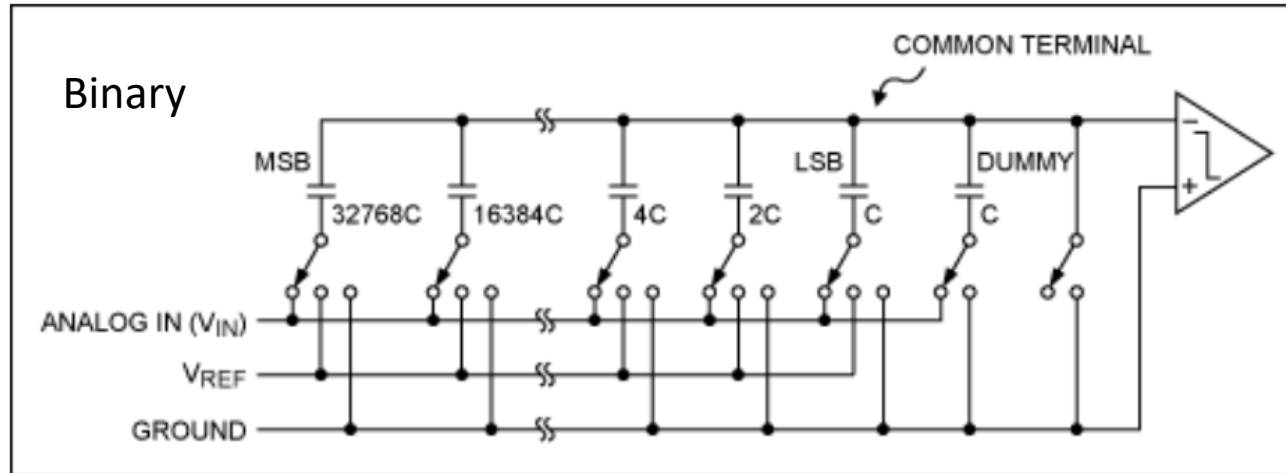
- Full array of capacitance
 - Binary
 - Hybrid Binary/Unary
- Capacitive array with Split array (cap attenuator)
- Capacitive array with 2C-C cells
- Hybrid Capacitive-resistive

With separate S&H

- Resistive (not good for very low power)

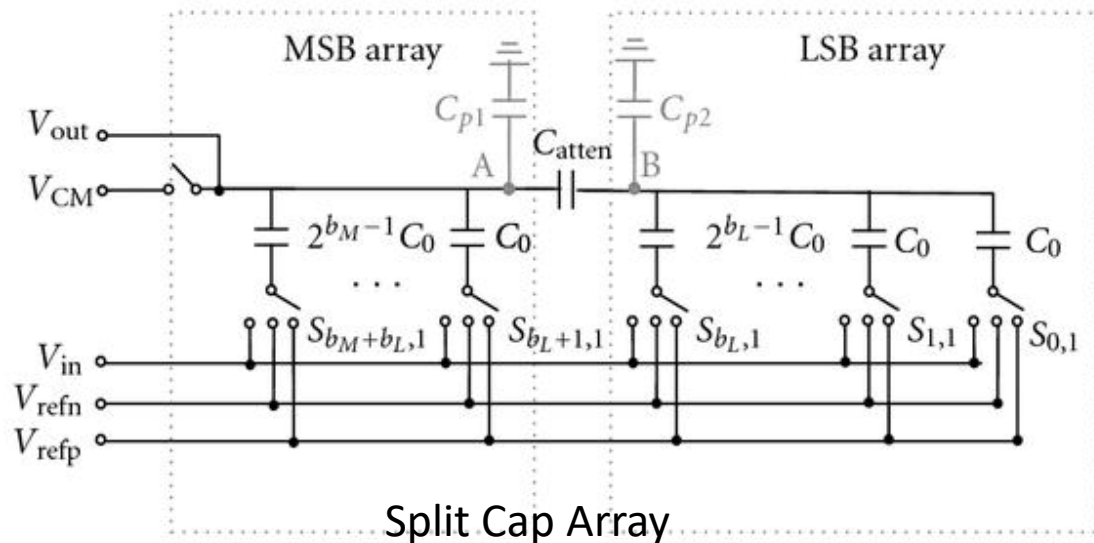
5.2 SAR Converters

SAR ARCHITECTURES



Unary all
unity elements

Hybrid
Binary/unary



The condition

yields the value of C_A

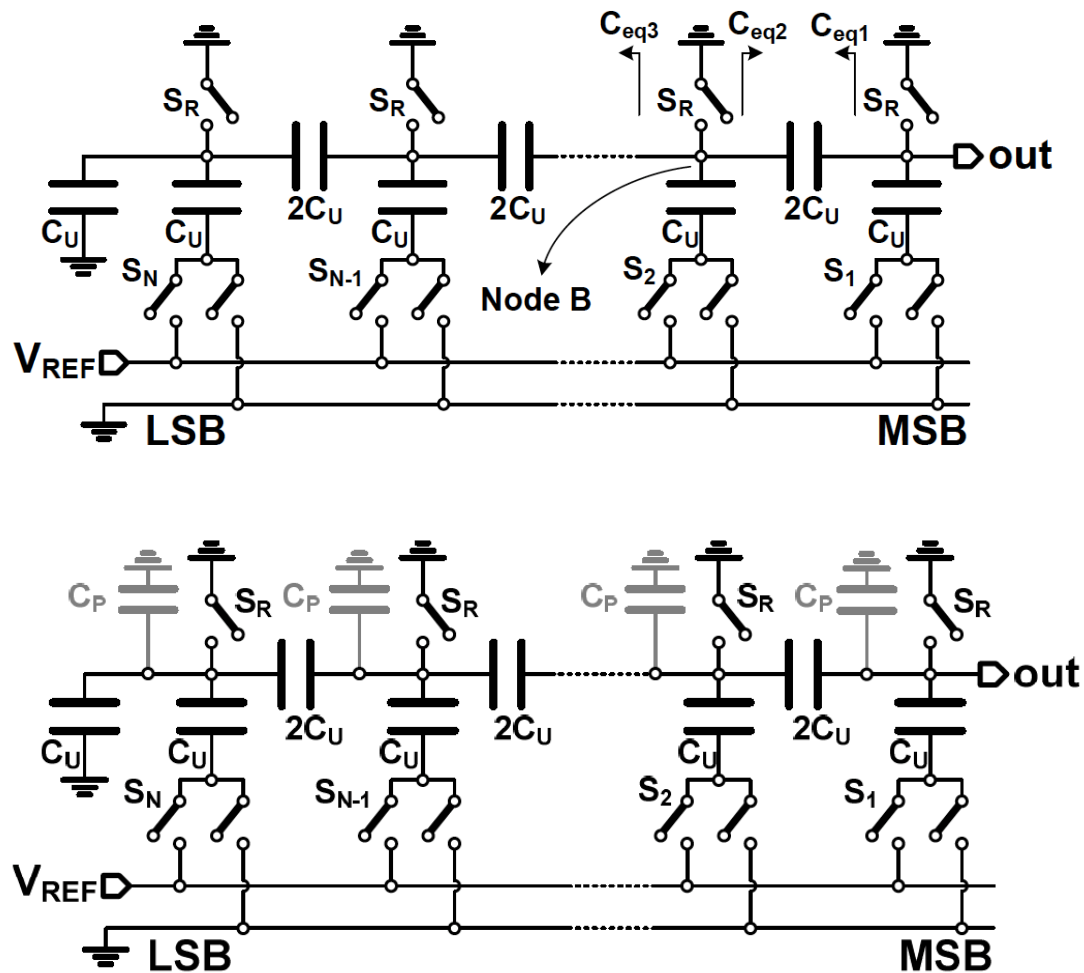
$$\frac{C_A \cdot 2^{n/2} C_U}{C_A + 2^{n/2} C_U} = C_u$$

$$C_A = \frac{2^{n/2}}{2^{n/2} - 1} C_U.$$

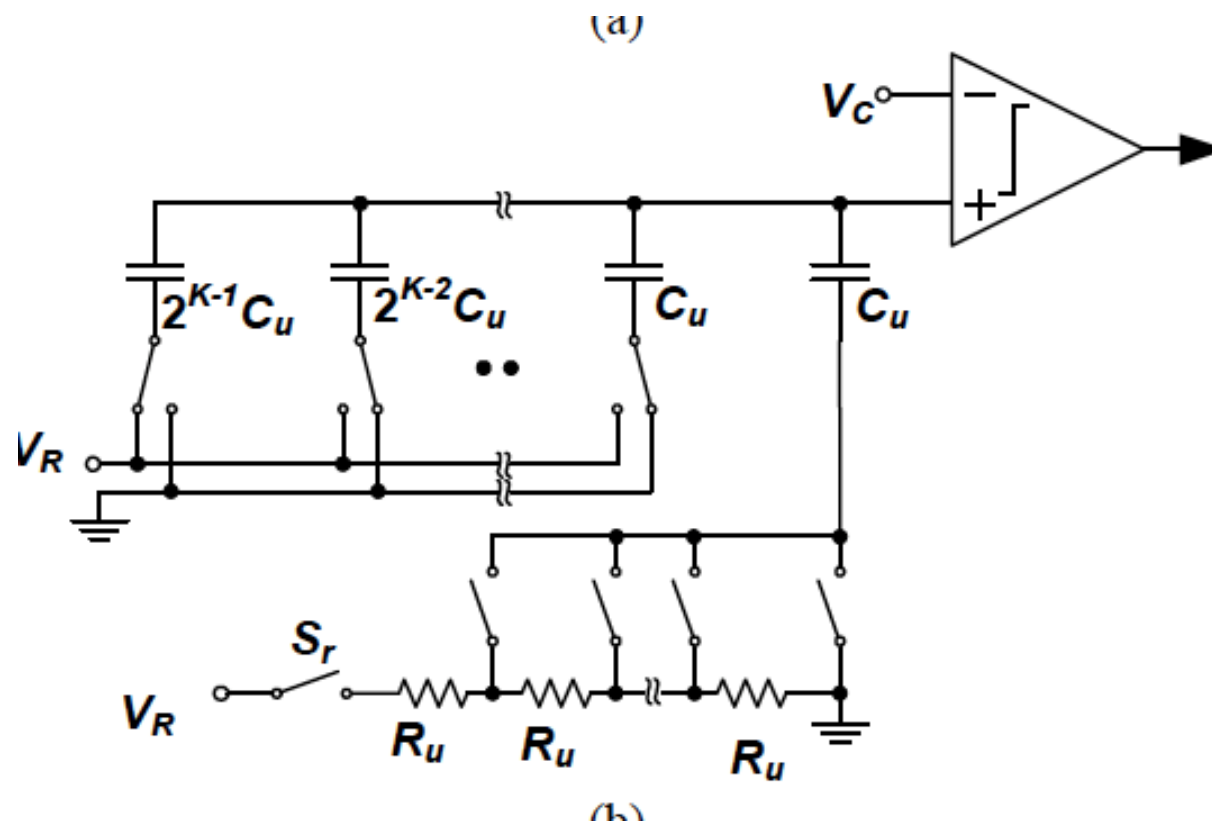
5.2 SAR Converters

2C – C Array

Parasitic limited



Hybrid Resistive Capacitive Array

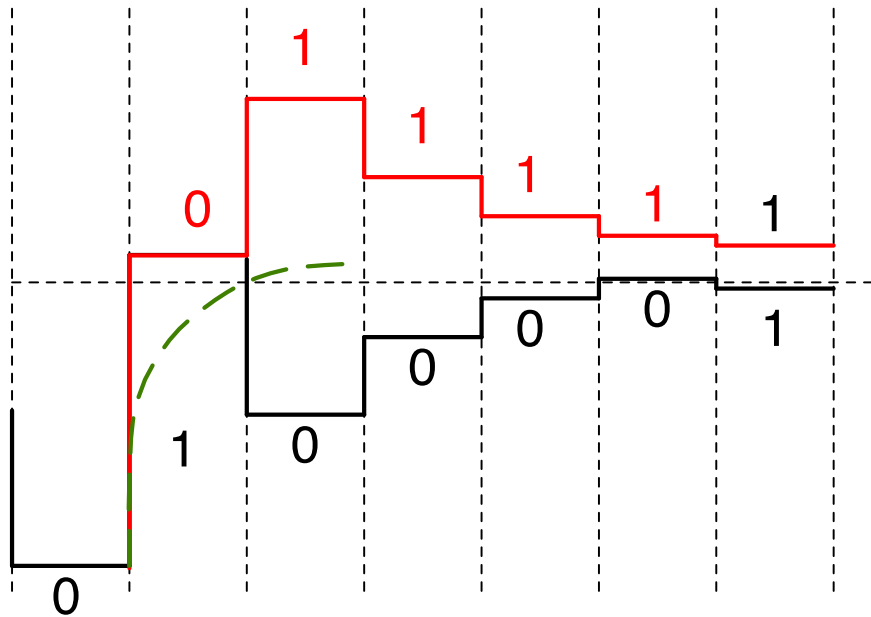


5.2 SAR Converters

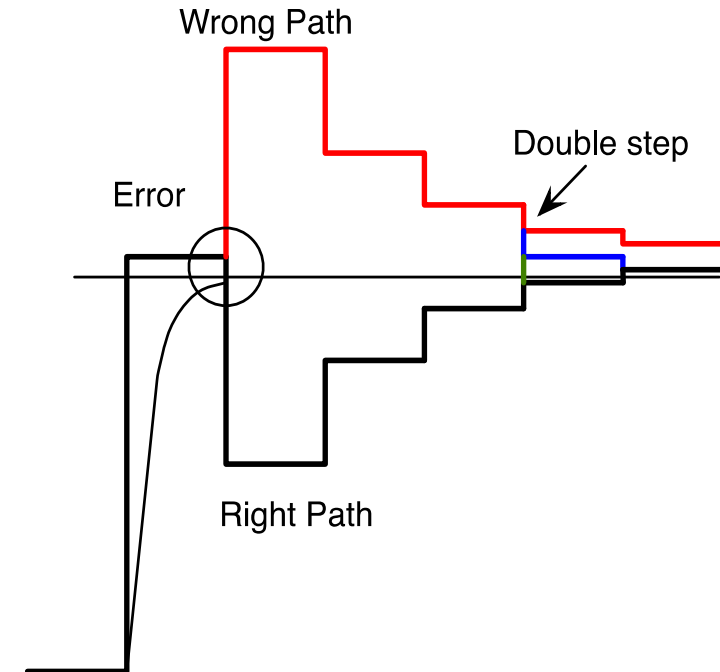
Search Error and Digital Correction

Comparator always able to resolve less than 1 LSB

- Critical at the beginning of the cycle



An early error in the search path is not recovered

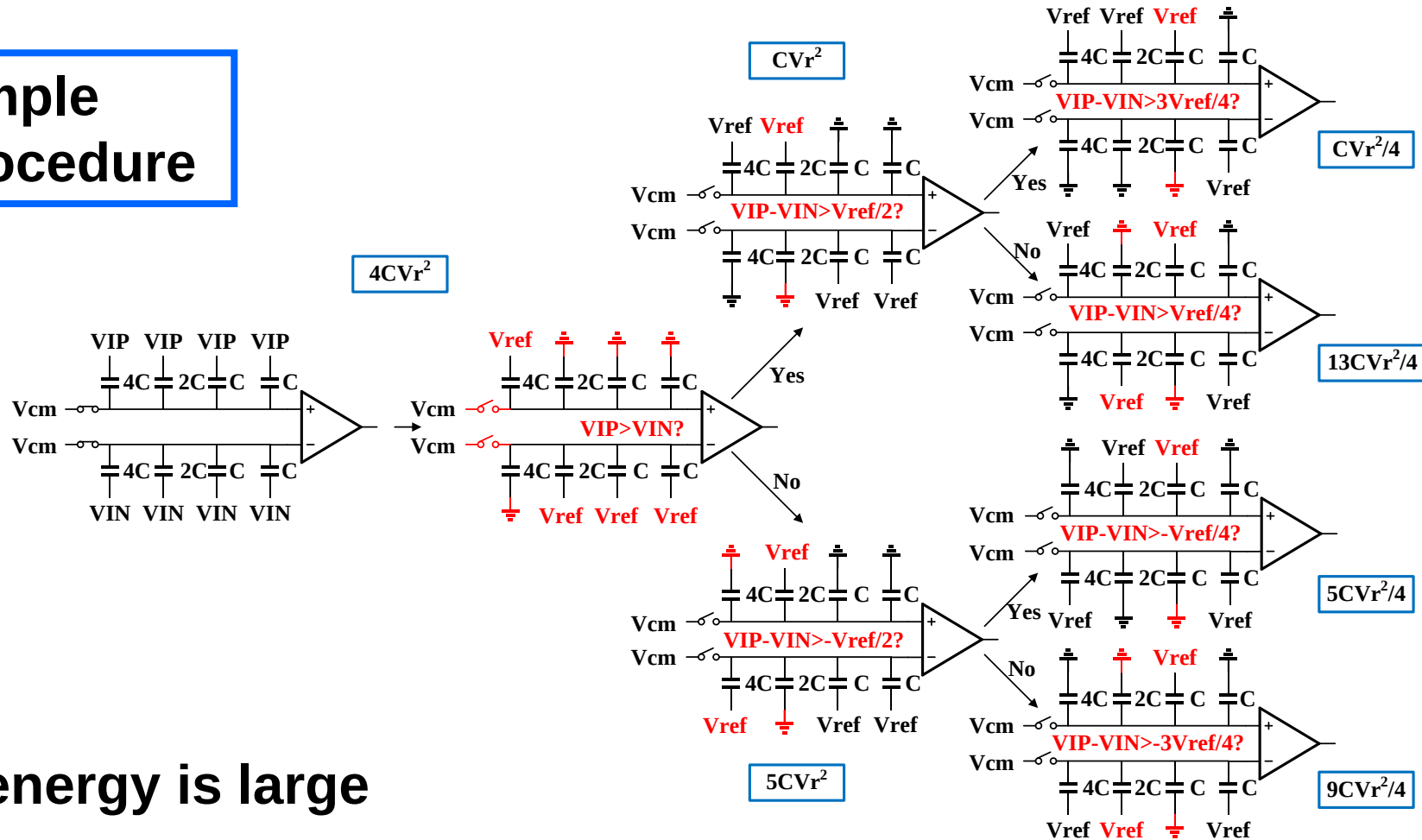


D. Gardino, F. Maloberti: "High Resolution Rail-To-Rail ADC in CMOS Digital Technology", ISCAS 1999, Vol. 2, pp. 339-342.

5.2 SAR Converters

Switching Power

3bit example Switching Procedure

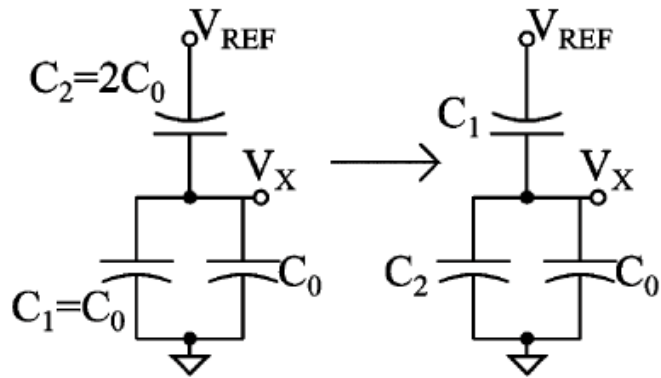


■ Switching energy is large

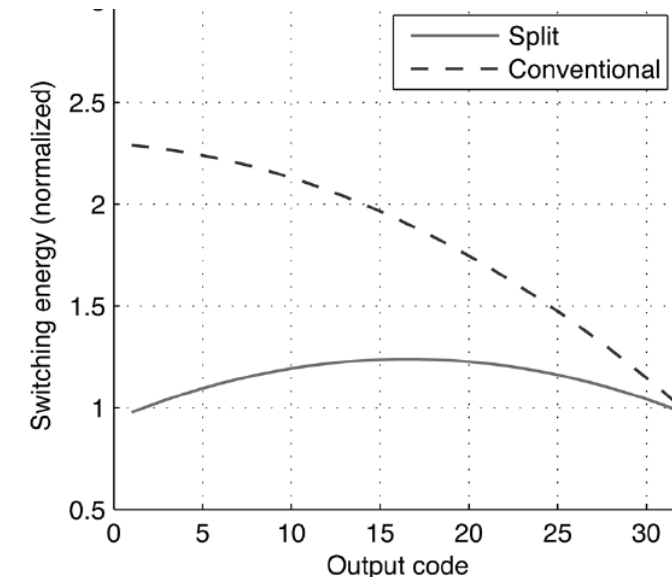
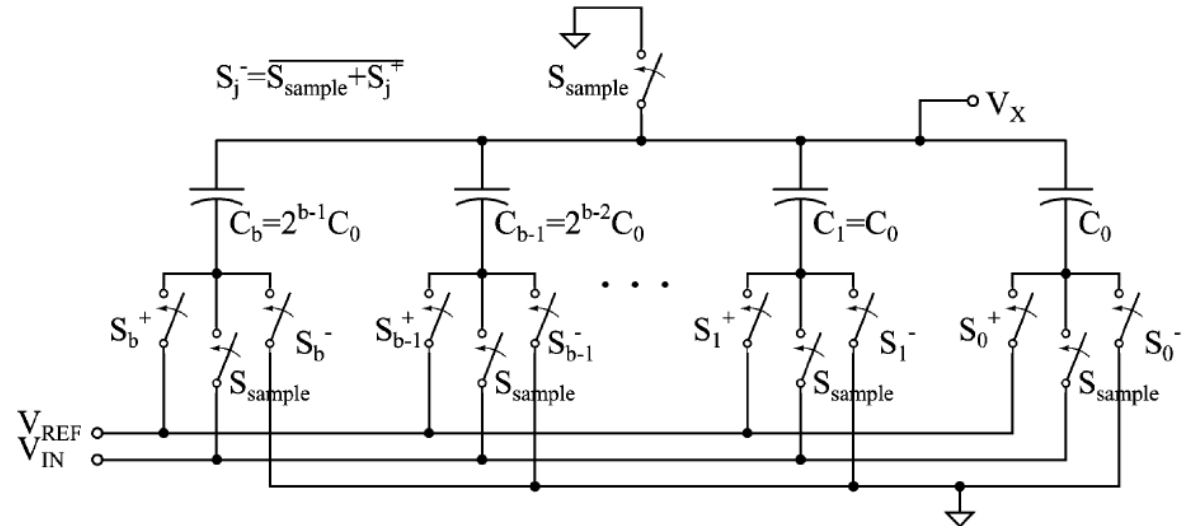
5.2 SAR Converters

Split-capacitor Switching Method

B.P. Ginsburg and A. Chandrakasan, "A MS/s 5-bit ADC in 65-nm CMOS With Split Capacitor Array DAC, *IEEE J. Solid-State Circuits*, pp. 739-747, 2004.



- ◆ Average saving 37%
- ◆ FoM 0.5 pJ/conversion

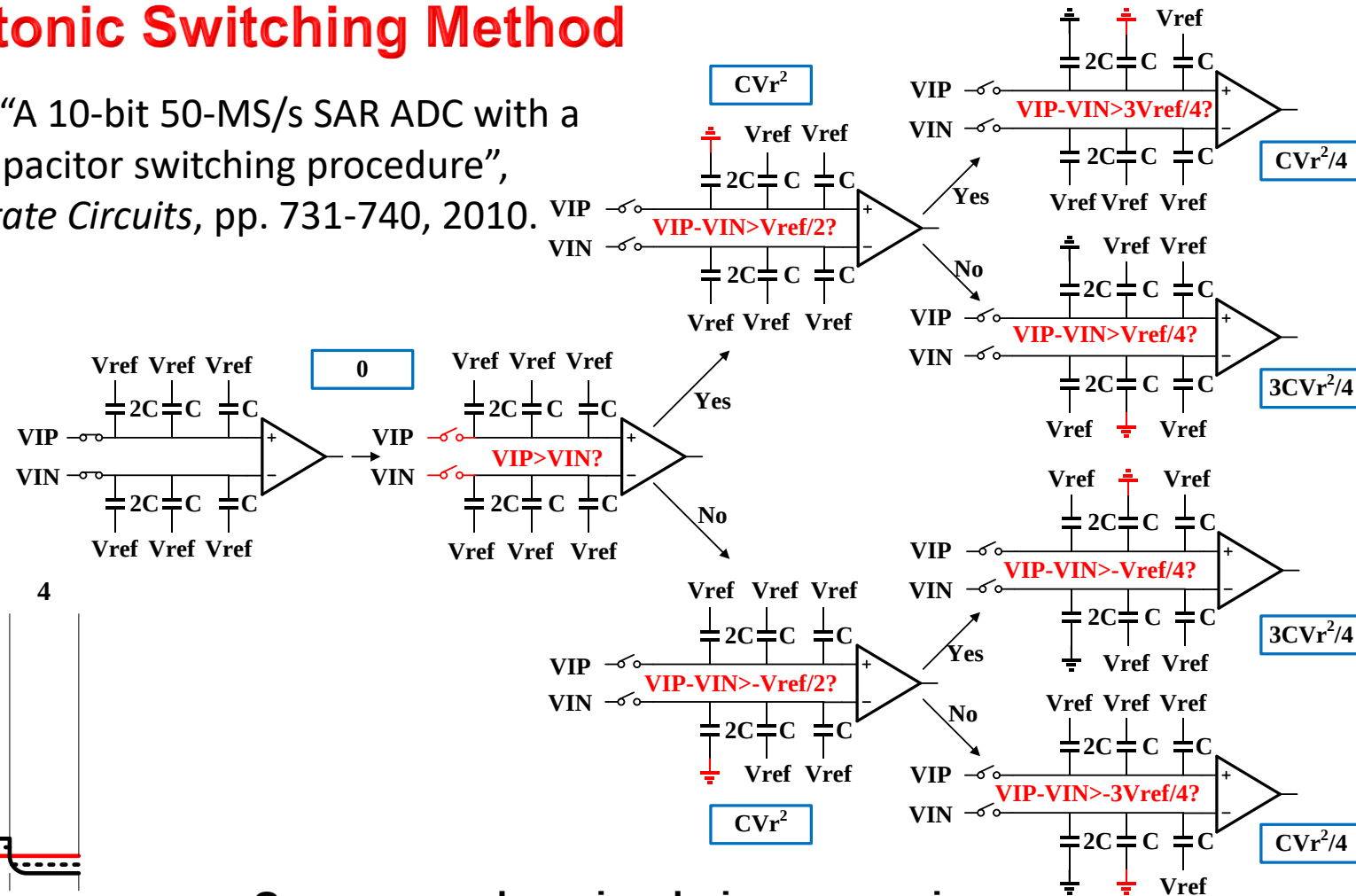
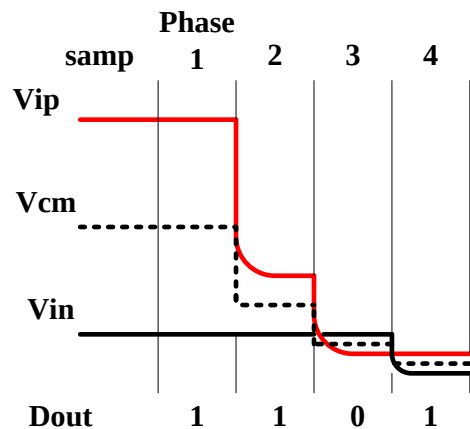


5.2 SAR Converters

Monotonic Switching Method

C.C.Liu, et al, "A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure", *IEEE J.Solid-State Circuits*, pp. 731-740, 2010.

FoM=52 fj

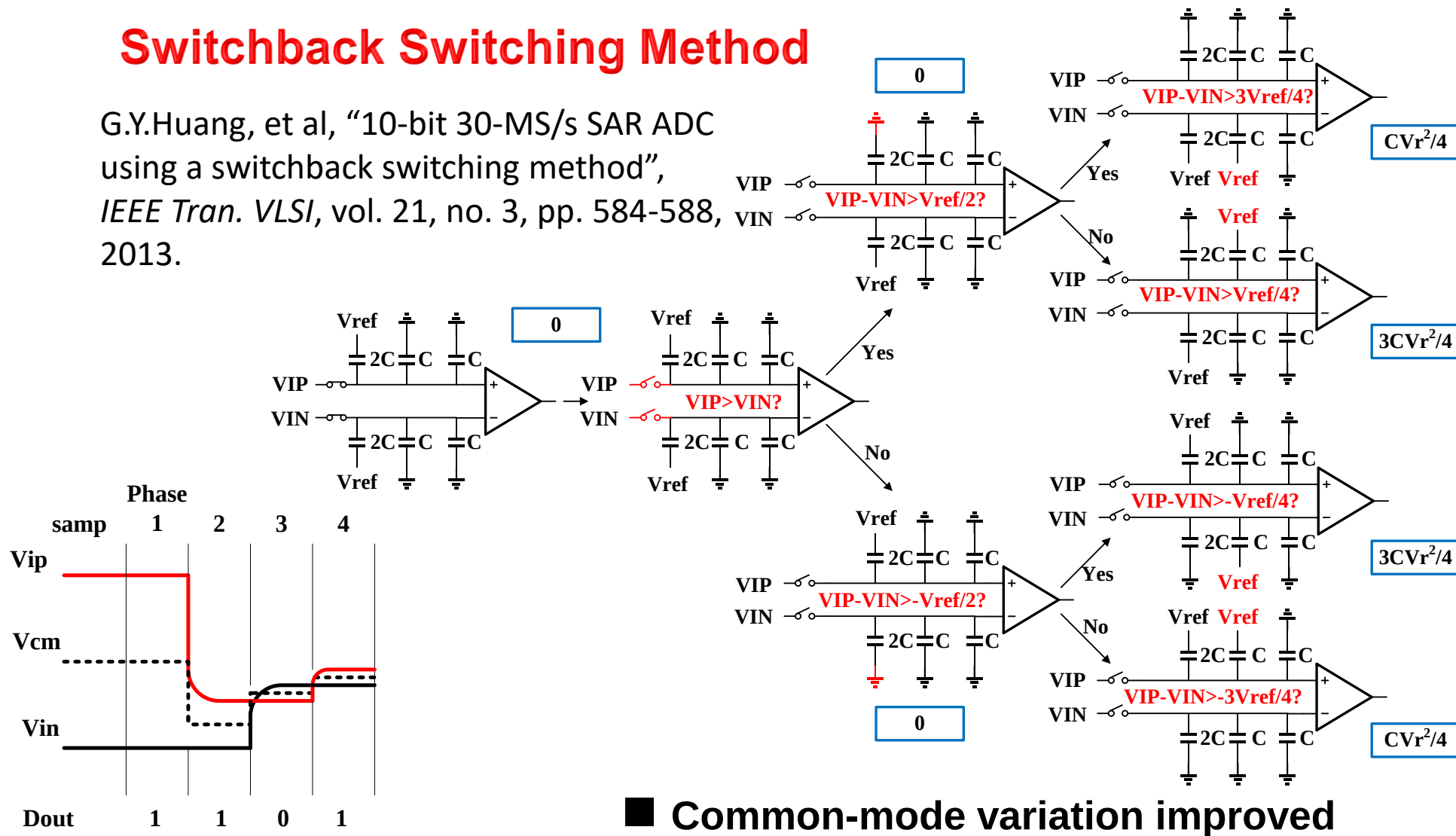


- Common-mode varies during conversion
- Degrade the conversion accuracy

5.2 SAR Converters

Switchback Switching Method

G.Y.Huang, et al, "10-bit 30-MS/s SAR ADC using a switchback switching method", *IEEE Tran. VLSI*, vol. 21, no. 3, pp. 584-588, 2013.

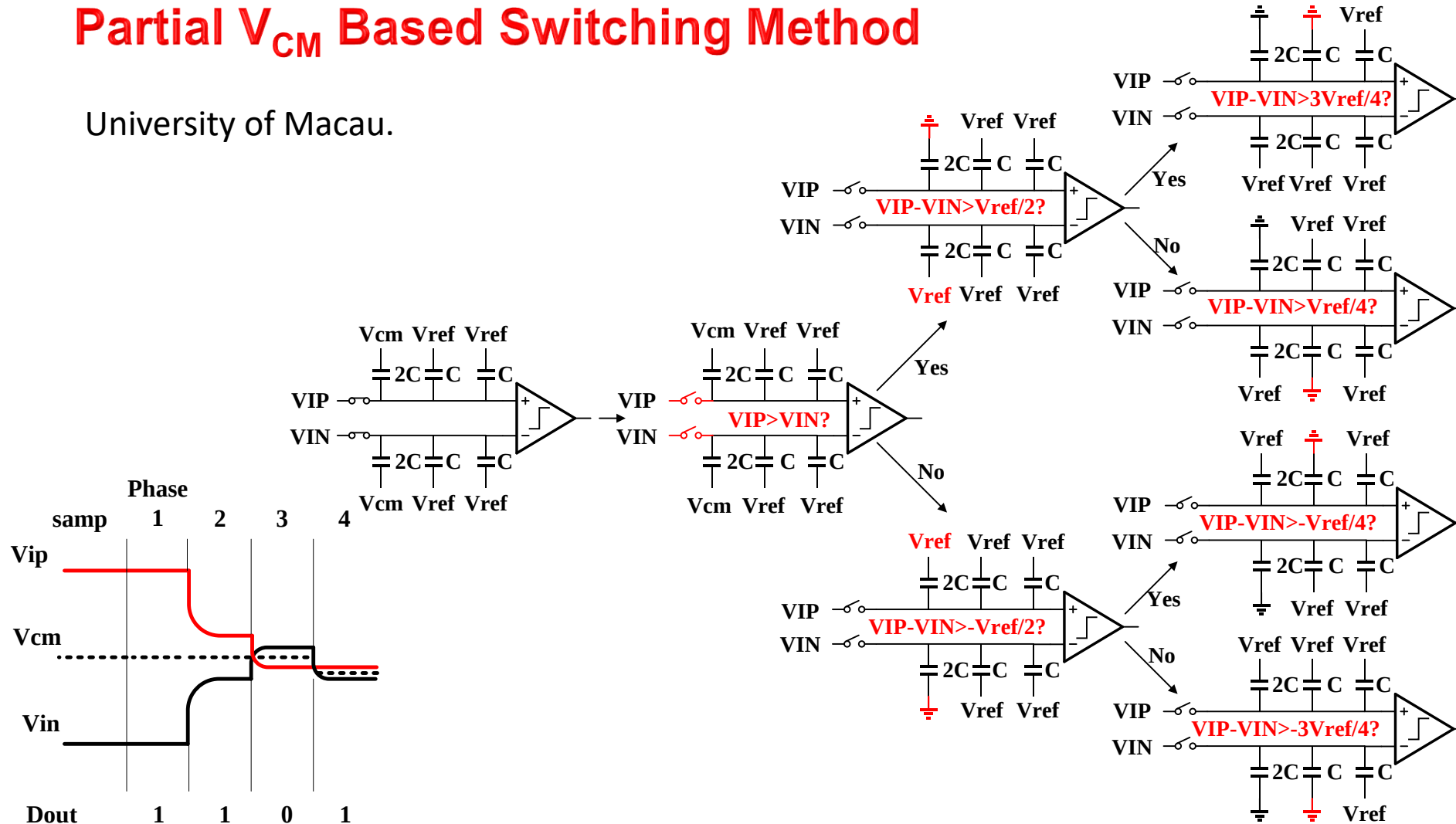


■ Common-mode variation improved

5.2 SAR Converters

Partial V_{CM} Based Switching Method

University of Macau.

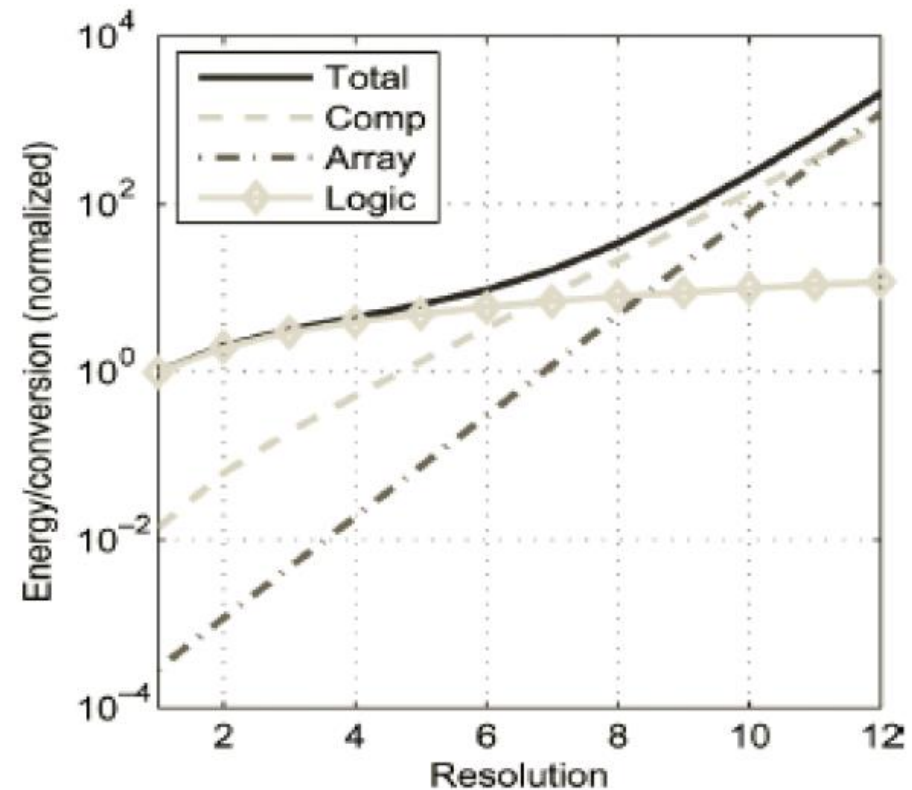


5.2 SAR Converters

- The power is for
 - Switching the capacitance array
 - Comparator
 - SAR logic

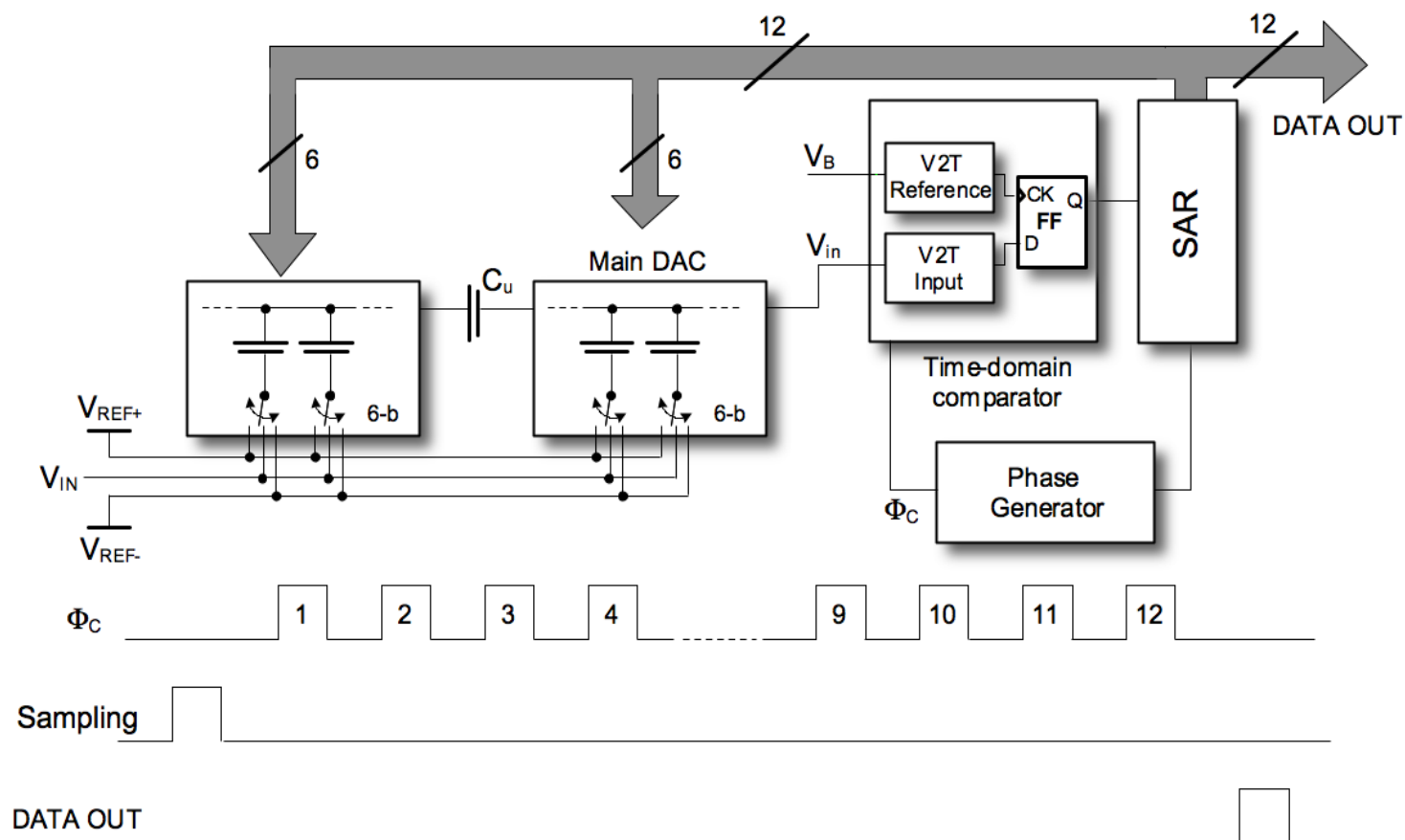
What we expect

Part	Power
Dynamic switching of caps	20
Comparator	40
Digital Logic	40



5.2 SAR Converters

DESIGN EXAMPLE 1



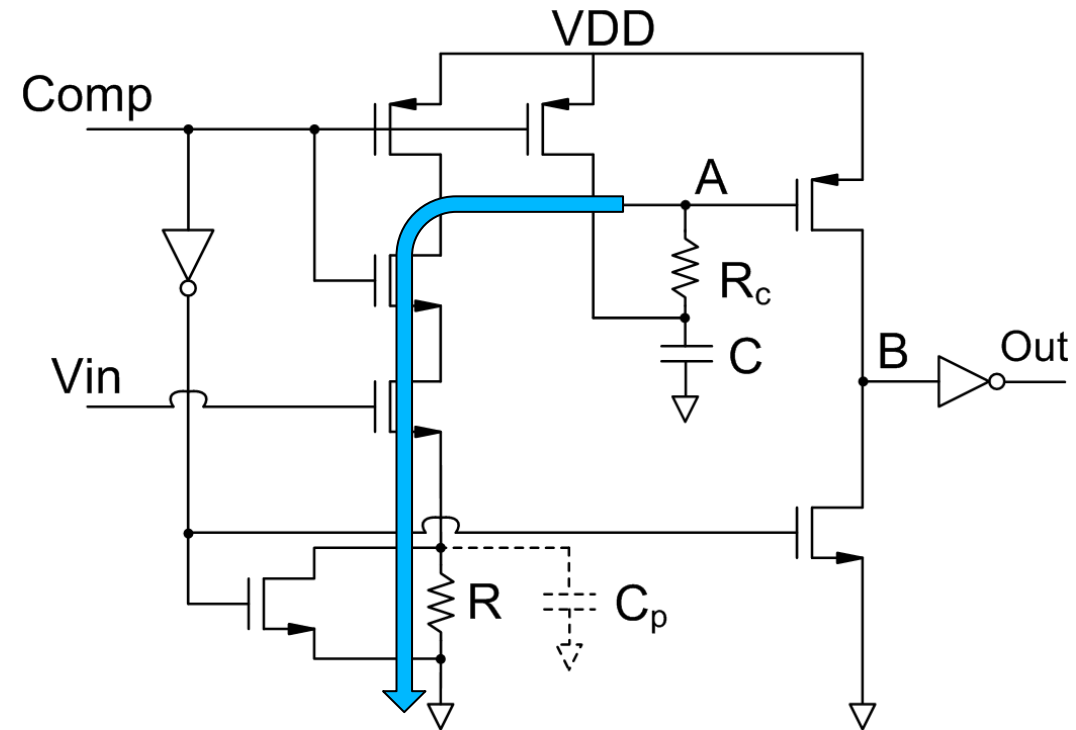
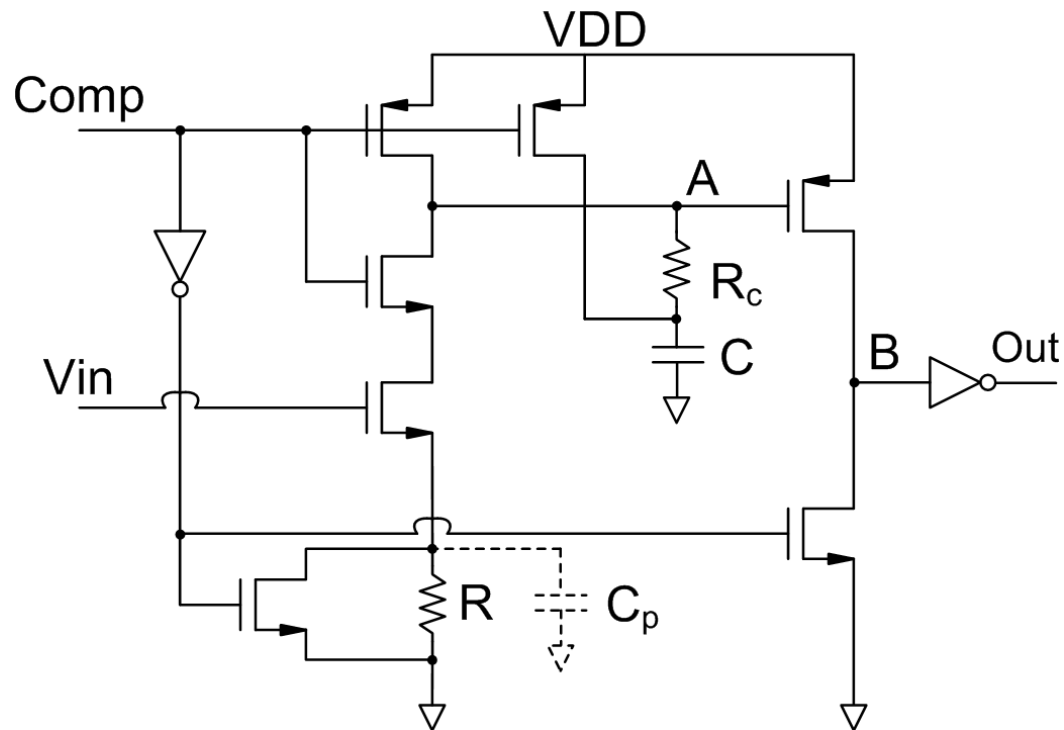
A 9.4-ENOB 1V 3.8 μ W
100kS/s SAR ADC with
Time-Domain Comparator

**A. Agnes, E. Bonizzoni, P. Malcovati, F. Maloberti:
ISSCC 2008, pp. 246-247.**

5.2 SAR Converters

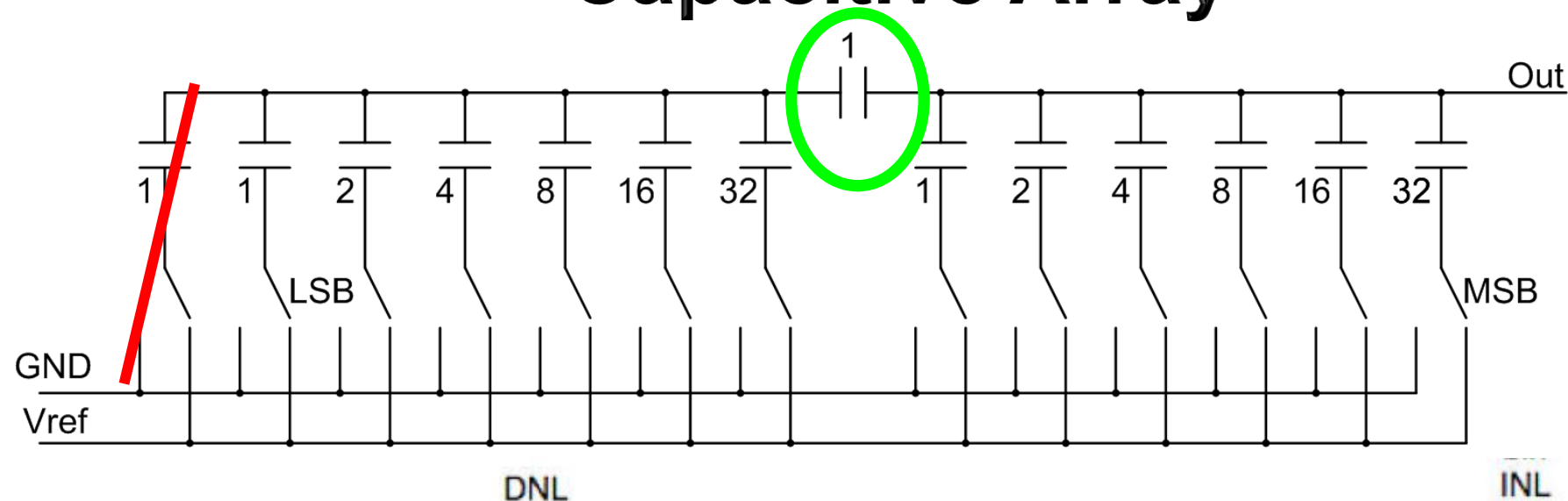
- Basic Building Block for Comparator
- Convert voltage level to current and then to time

- Technology: National 70 cmos9 (0.18 μm)
- Comparator Response Time about 250 ns

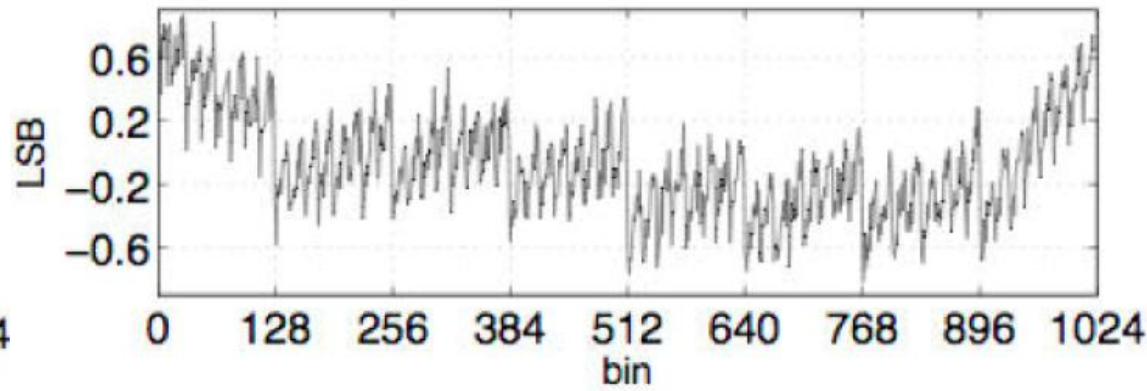
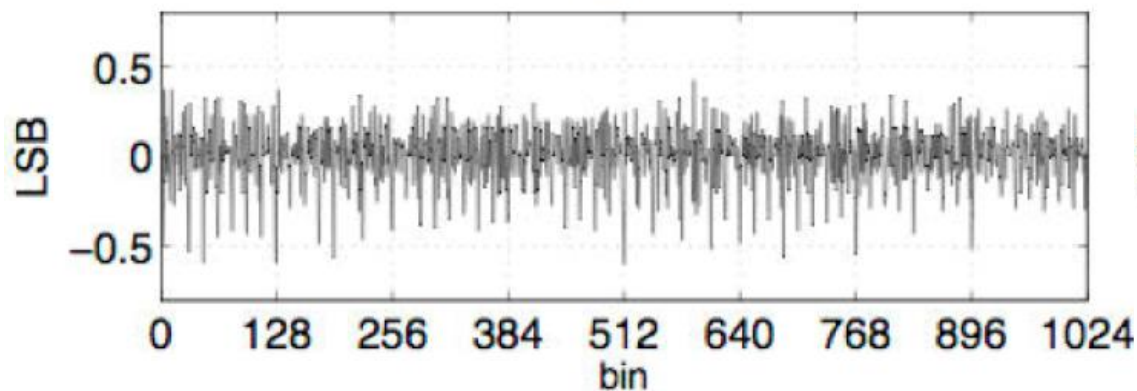


5.3 SAR Converters

Capacitive Array



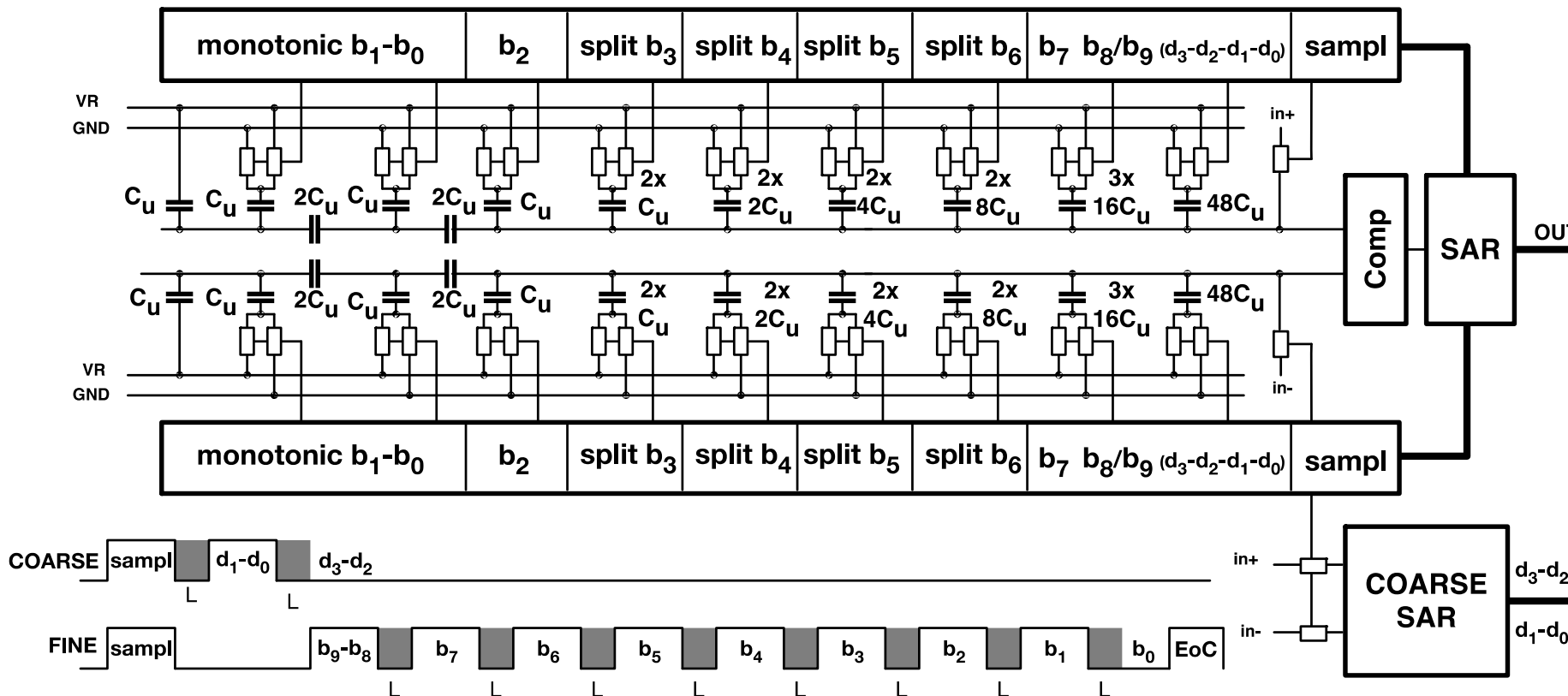
FoM= 56 fJ/conv-lev



5.2 SAR Converters

DESIGN EXAMPLE 2: Coarse and fine SAR

- Use an auxiliary ADC for the first bits (coarse/fine)

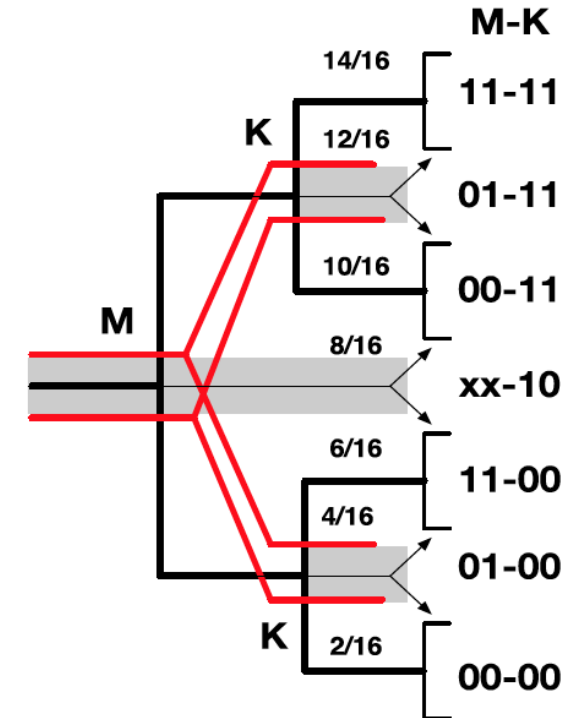
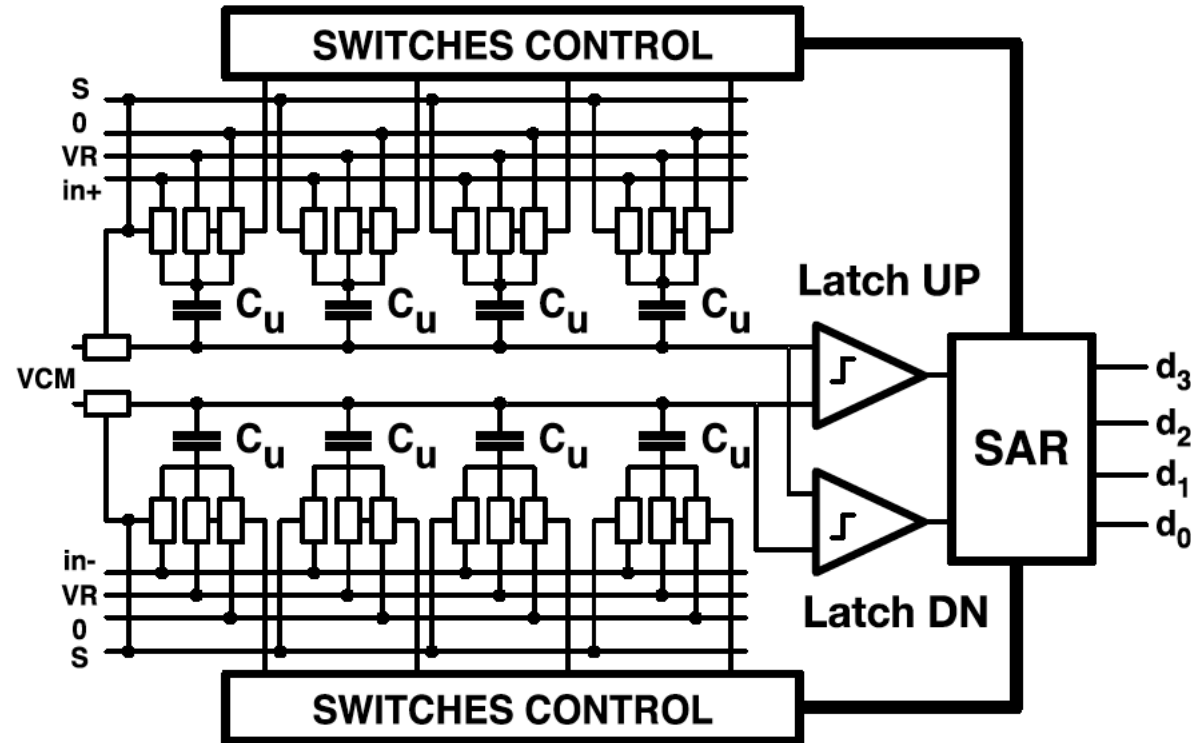


Y. Zhang, E. Bonizzoni, and F. Maloberti, "A 10-bit, 200-kS/s, 250-nA Self-Clocked Coarse-Fine SAR ADC", IEEE Transactions on Circuits and Systems II: Express Briefs, pp- 924-928, 2016

(FoM=1.88 fJ/conv)

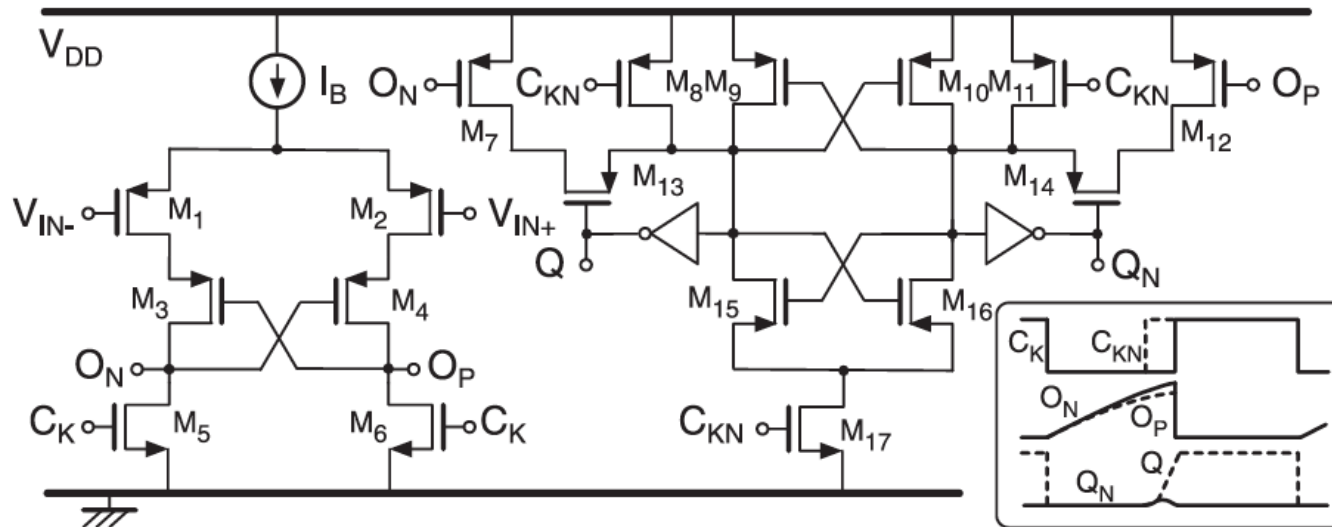
5.2 SAR Converters

- Auxiliary SAR with very small unity capacitors; two latches with shifted thresholds

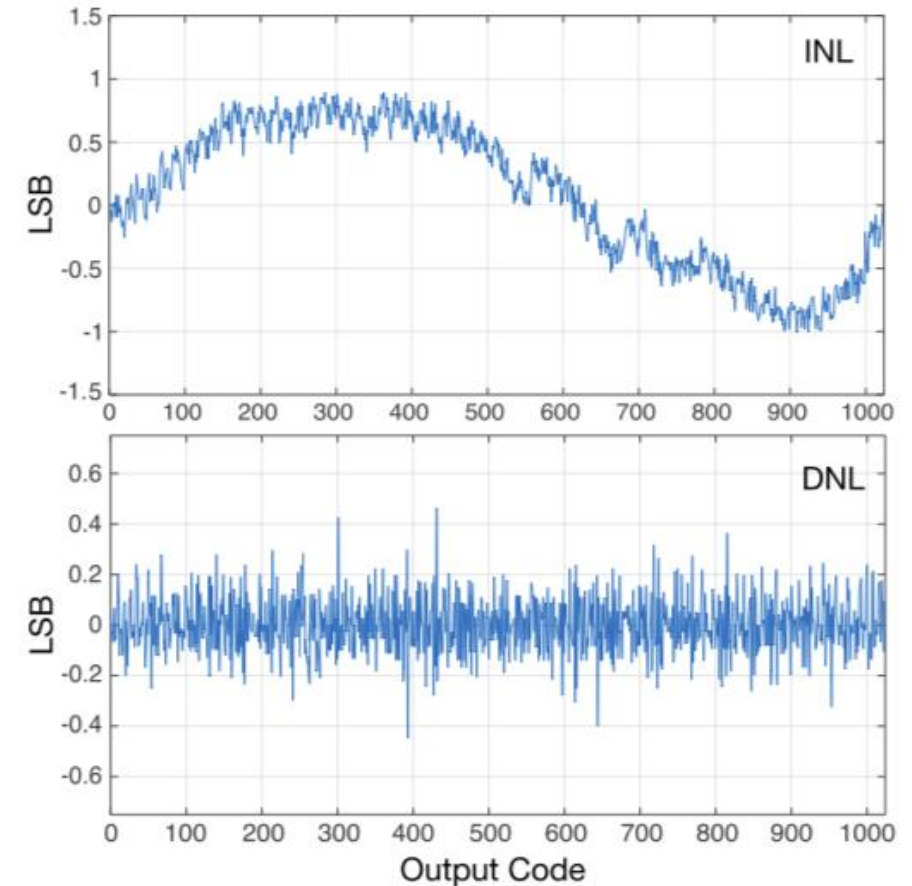


5.2 SAR Converters

- Switching energy competitive with top plate sampling
- Dynamic pre-amp (2nA)

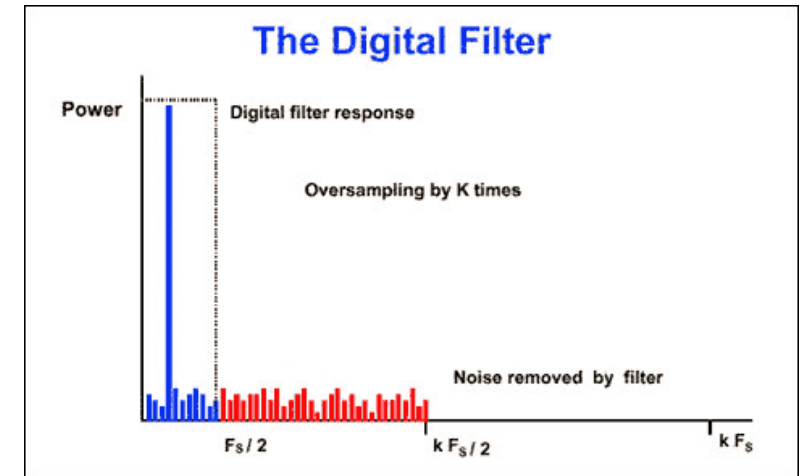
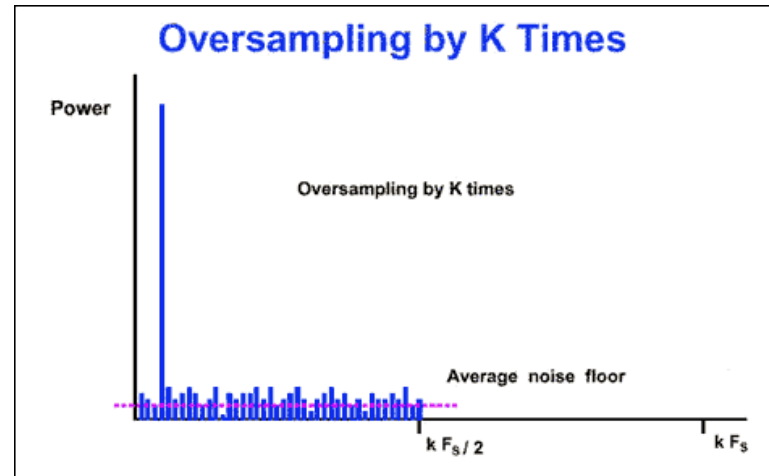
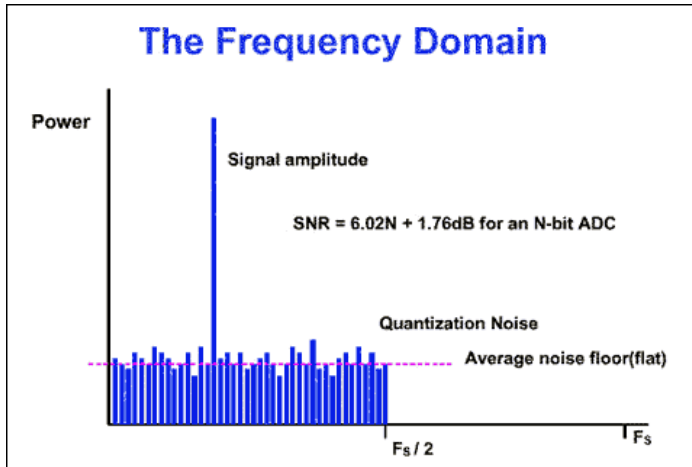


Power breakdown is 130 nA for the analog (comparator, DAC switching, and sampling clock-boosted switches) and 120 nA for the digital part.



5.3 Sigma Delta and Incremental Converters

BENEFITS OF OVERSAMPLING



$$N_{\sigma_{e_Q}^2} = \int_{-f_B}^{+f_B} S_{e_Q}(f) df = \int_{-f_B}^{+f_B} \frac{V_{LSB}^2}{12 \cdot f_s} df = \frac{2 \cdot f_B V_{LSB}^2}{12 \cdot f_s} = \frac{V_{LSB}^2}{12 \cdot OSR}$$

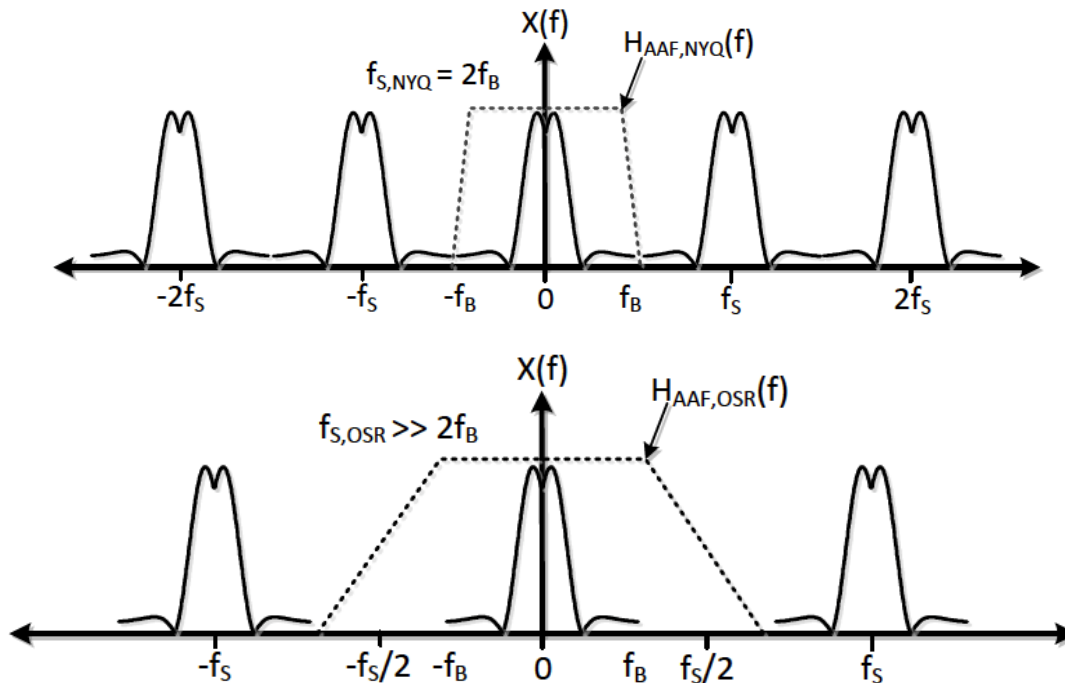
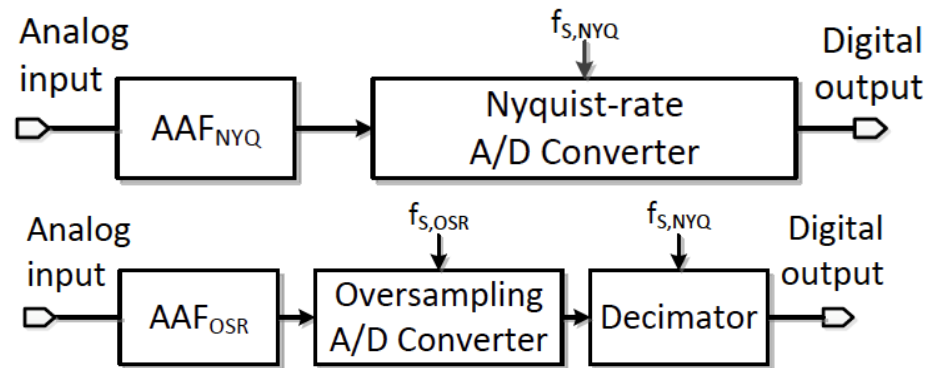
$$SQNR_{SIN} [dB] = 10 \log_{10} \left(\frac{P_{SIN}}{N_{\sigma_{e_Q}^2}} \right) = 10 \log_{10} \frac{(2^{N_B} \cdot V_{LSB})^2}{8} \frac{12 \cdot OSR}{V_{LSB}^2}$$

$$1\text{-bit} \rightarrow 6.02 \text{ dB}$$

$$\approx 6.02 \cdot N_B + 10 \log_{10} OSR + 1.76.$$

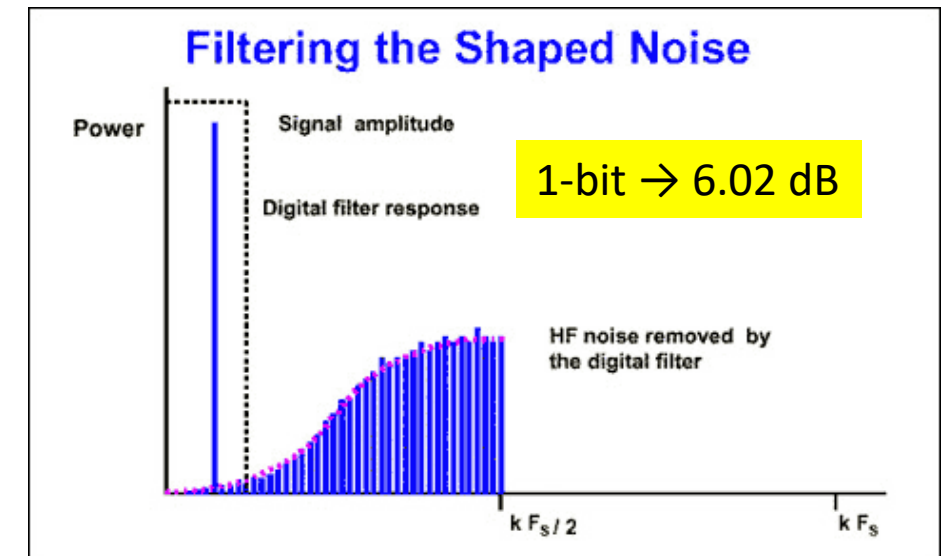
$$10 \log_{10} OSR = 3.01 \log_2 OSR$$

5.3 Sigma Delta and Incremental Converters



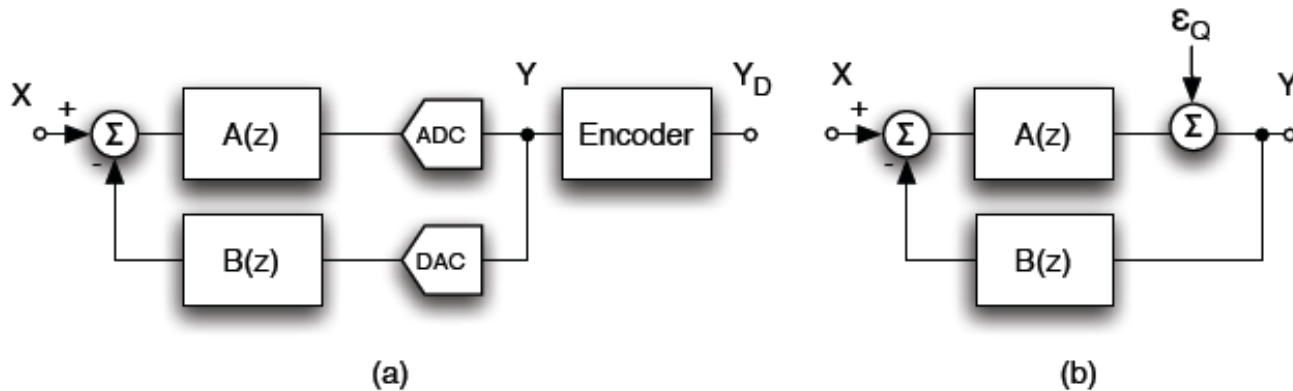
How to improve the SNR and, consequently, increase the equivalent number of bits?

- Reduce the quantization noise in the band of interest.
- Shape the noise spectrum.



5.3 Sigma Delta and Incremental Converters

How to obtain noise shaping?



$$Y = \frac{X \cdot A(z)}{1 + A(z)B(z)} + \frac{\epsilon_Q}{1 + A(z)B(z)}$$

$$Y = X \cdot S(z) + \epsilon_Q \cdot N(z)$$

$B(z)$ can simply be equal to 1;

$A(z)$ should be integration-type. $\rightarrow \frac{z^{-1}}{1-z^{-1}}$

Place the quantizer in a feedback loop.

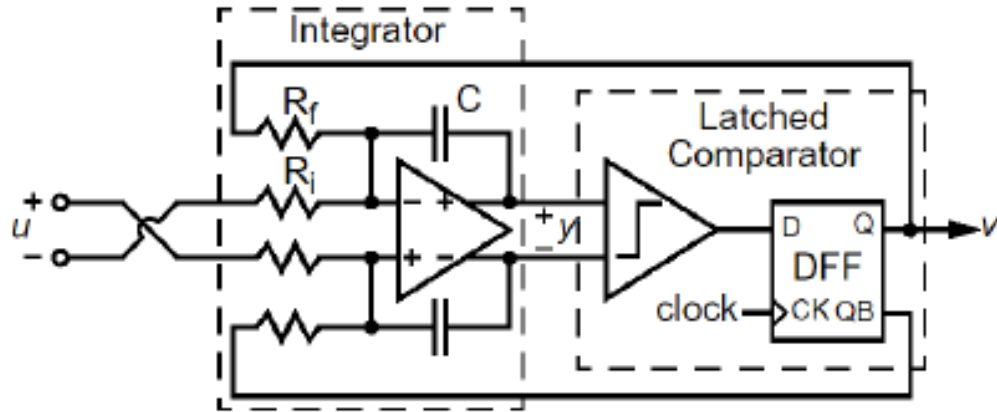
The system has two inputs (signal and noise) and one output.

Goal is to have different suitable transfer functions (STF = signal TF, and NTF = Signal TF).

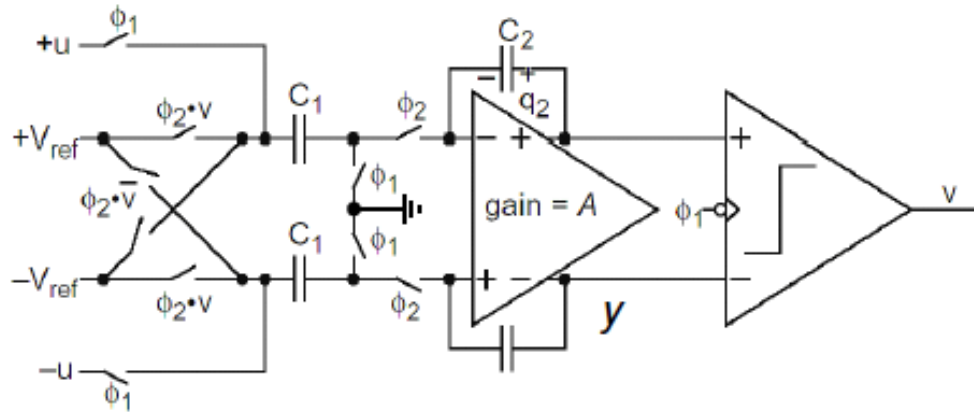
$$[X - Y \cdot B(z)] A(z) + \epsilon_Q = Y,$$

5.3 Sigma Delta and Incremental Converters

Fully Differential Continuous-time



Fully Differential Discrete-time



STF and NTF of the First Order Modulator

$$H(z) = \frac{z^{-1}}{1 - z^{-1}}$$

$$Y(z) = \{X(z) - Y(z)\} \frac{z^{-1}}{1 - z^{-1}} + \epsilon_Q(z)$$

$$Y(z) = X(z) \cdot z^{-1} + \epsilon_Q(z)(1 - z^{-1})$$

$$Y(z) = X \cdot STF(z) + \epsilon_Q(z) \cdot NTF(z).$$

The STF is a simple delay (more than what we desire).

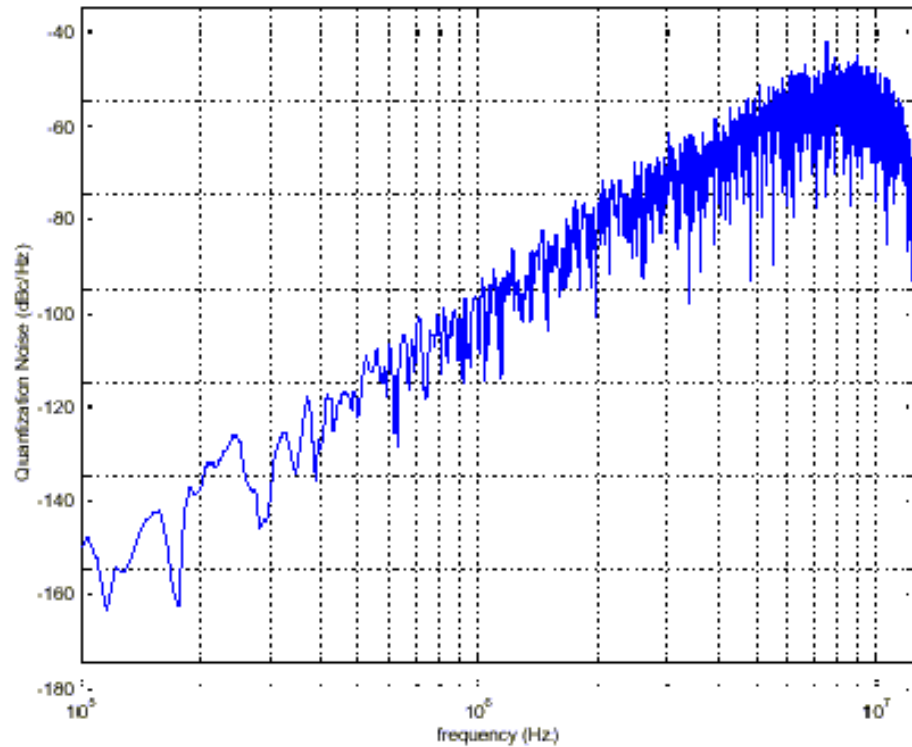
The NTF is $(1 - z^{-1})$, that using the $z \rightarrow s$ transformation becomes

$$NTF(\omega) = 1 - e^{-j\omega T} = 2je^{-j\omega T/2} \frac{e^{j\omega T/2} - e^{-j\omega T/2}}{2j}$$

$$NTF(\omega) = 2je^{-j\omega T/2} \sin(\omega T/2)$$

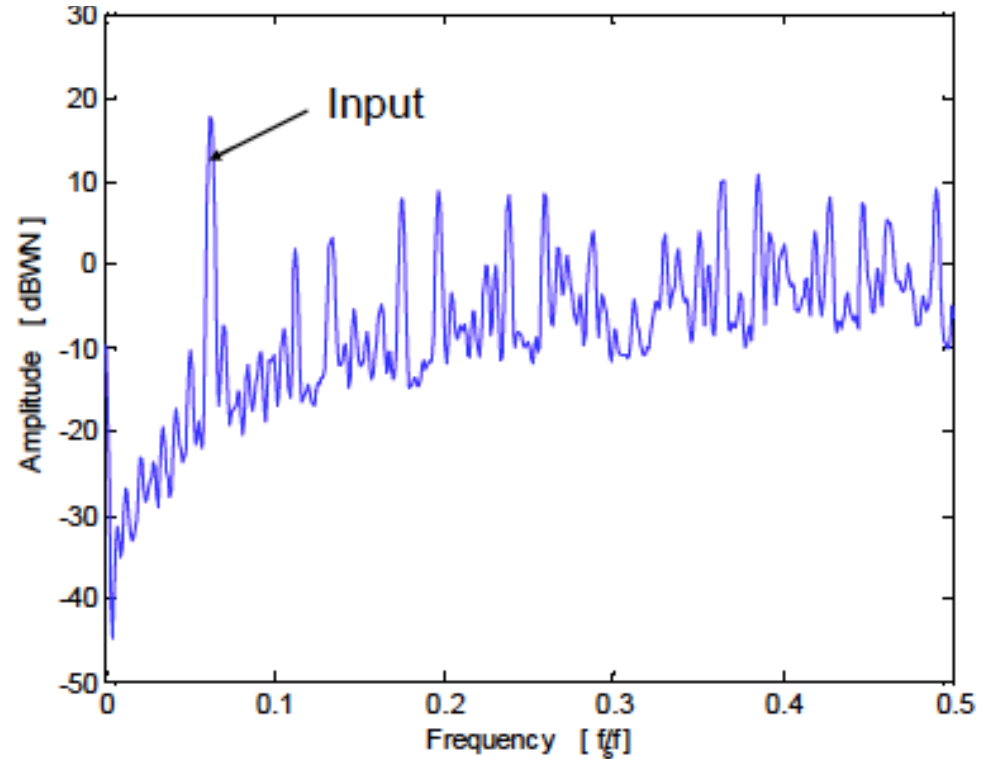
5.3 Sigma Delta and Incremental Converters

Spectrum of the quantization Noise $0 - f_s$



Ideal dB - log scale

Spectrum of the quantization Noise $0 - f_s/2$



Real dB – linear scale

5.3 Sigma Delta and Incremental Converters

What matter is the power of the shaped quantization noise in the signal band

$$V_n^2 = v_{n,Q}^2 \int_0^{f_B} 4 \cdot \sin^2(\pi f T) df \simeq v_{n,Q}^2 \frac{4\pi^2}{3} f_B^3 T^2$$

$$V_n^2 = V_{n,Q}^2 \frac{\pi^2}{3} \left[\frac{f_B}{f_s/2} \right]^3 = V_{n,Q}^2 \frac{\pi^2}{3} \cdot OSR^{-3}$$

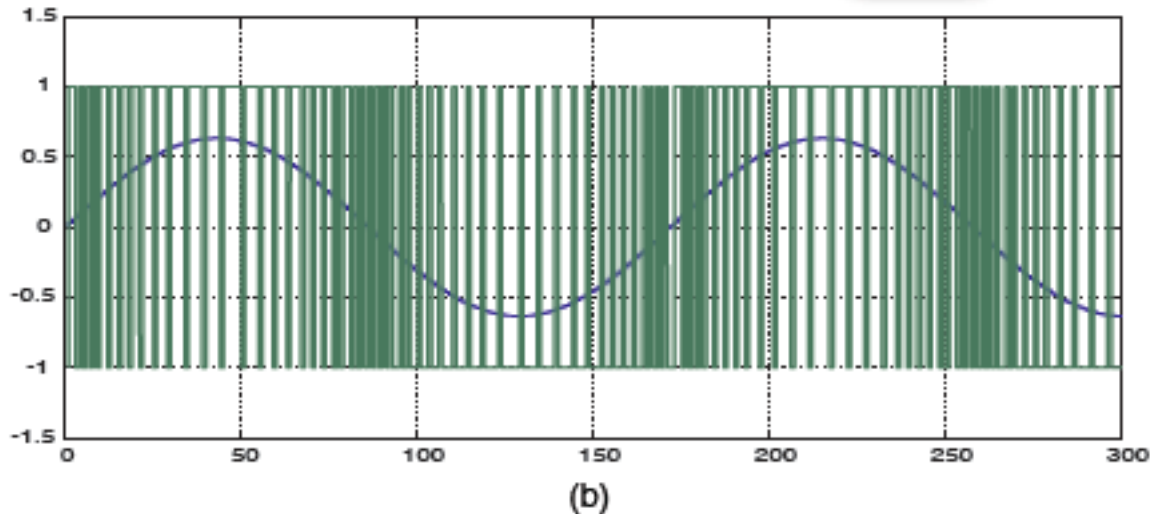
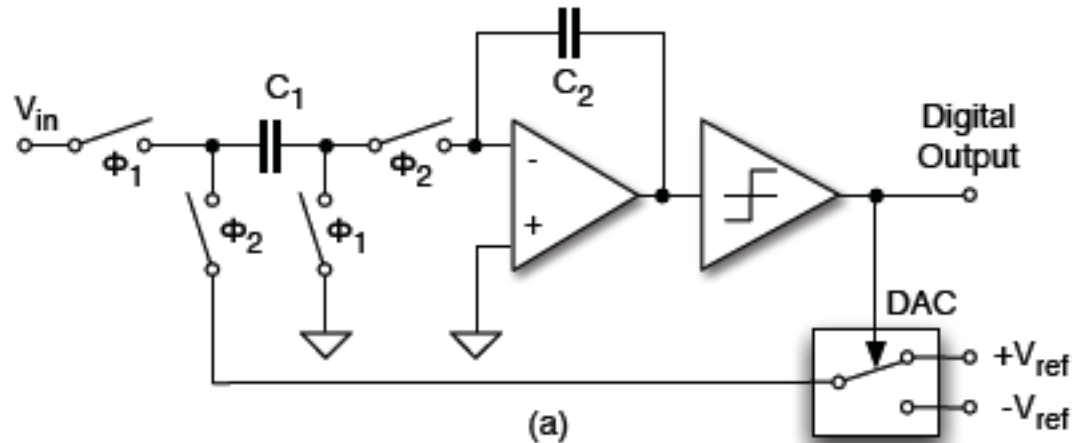
Leading to the SNR:

$$SNR_{\Sigma\Delta,1}|_{dB} = 6.02 \cdot n' + 1.78 - 5.17 + 9.03 \cdot \log_2(OSR)$$

Where $n' = \log_2 k$ k is the number of quantization intervals

Since 6.02 dB correspond to 1-bit the EQB increases by 1.5 bit every doubling of OSR

5.3 Sigma Delta and Incremental Converters

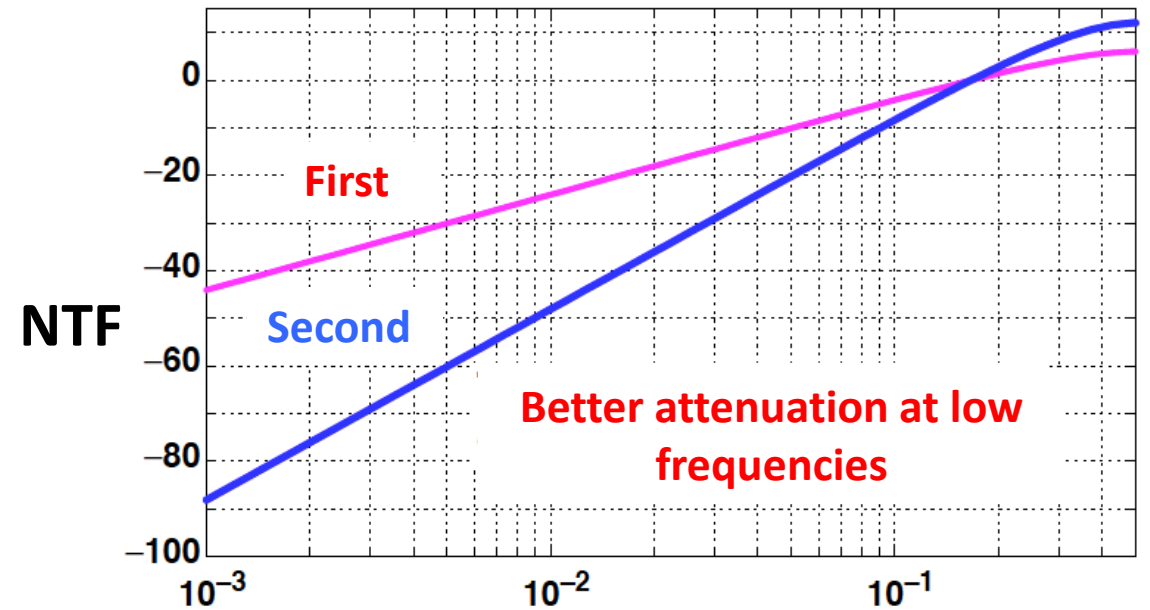


SINGLE BIT QUANTIZER IS A CHOICE

1 integrator in the loop grants 1.5 bit every doubling of OSR
 2 integrators in the loop grants 2.5 bit every doubling of the OSR

$$Y(z) = X(z) z^{-1} + E(z) (1 - z^{-1})^2$$

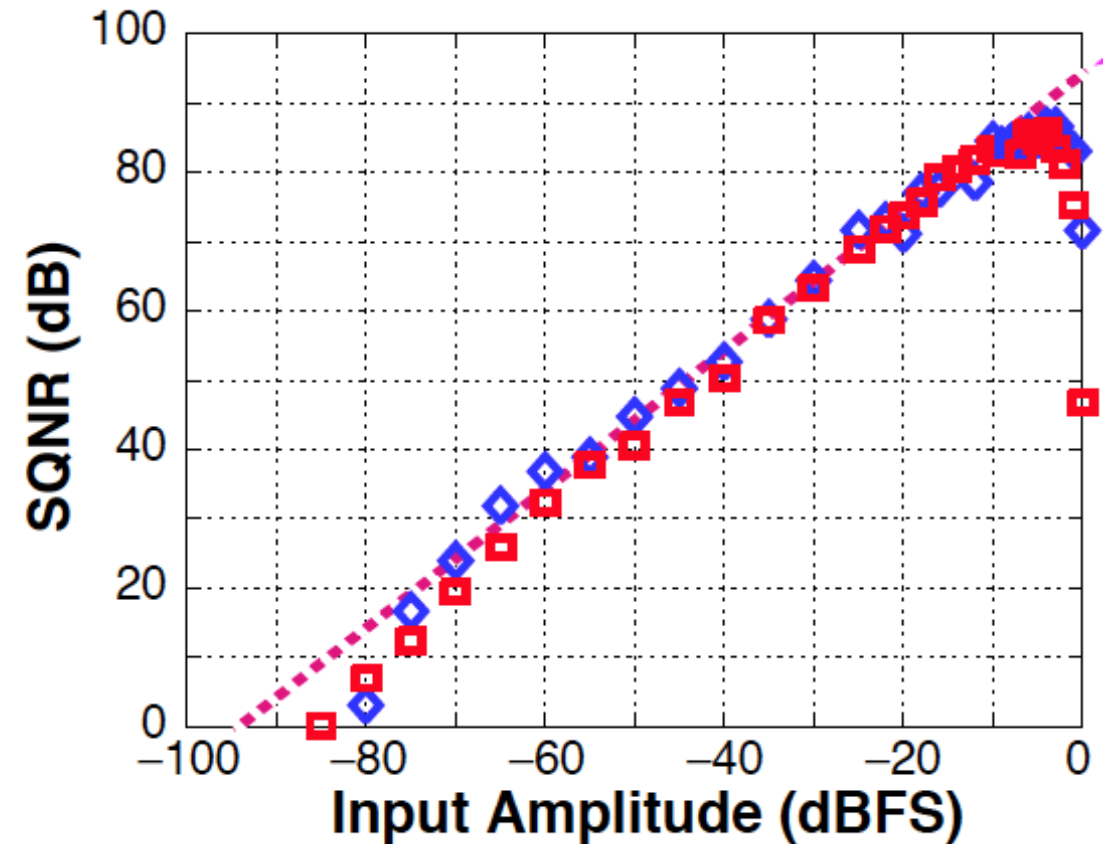
$$SNR_{\Sigma\Delta_2}|_{dB} = 6.02n' + 1.78 - 12.9 + 15.05 \cdot \log_2(OSR)$$



5.3 Sigma Delta and Incremental Converters

NOTICE THAT

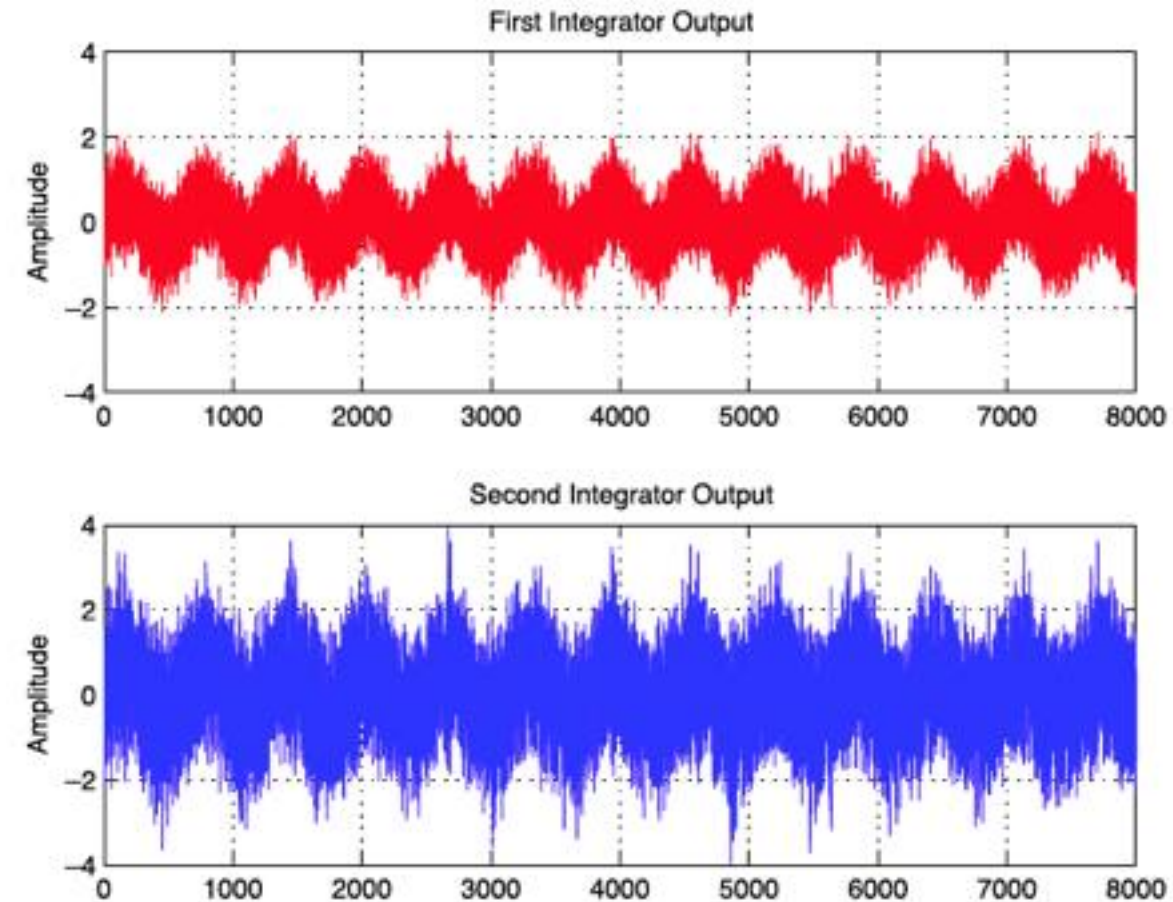
1. With a first order modulator there are big tones, especially with slow signals.
2. Having two integrators around the loop causes oscillations. Some simple actions are necessary
3. More than two integrator around the loop are problematic and making the scheme stable “costs”.
4. When the signal is close to the full scale the SNR drops. The peak SNR differs from the DR.



5.3 Sigma Delta and Incremental Converters

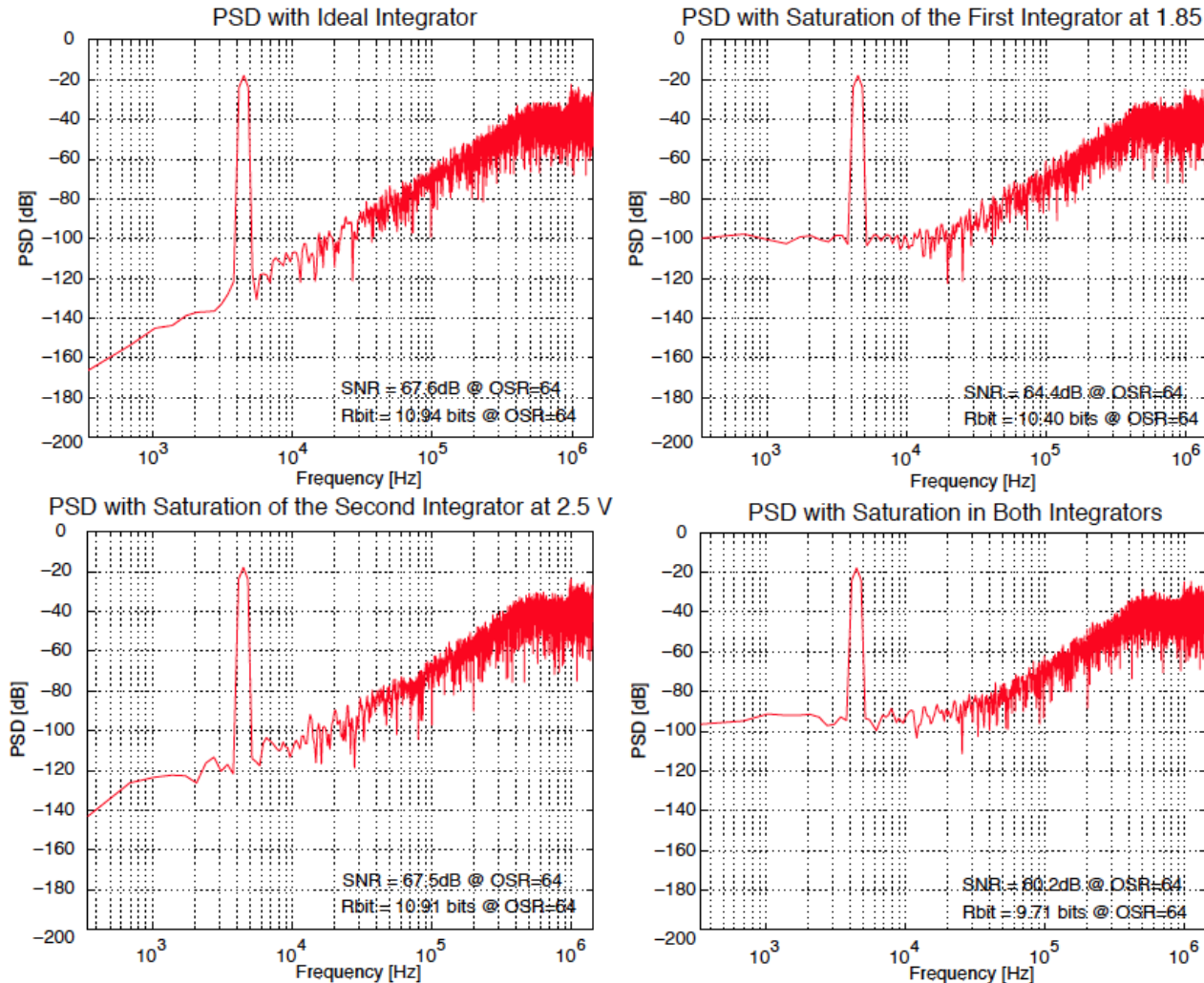
NOTICE THAT

1. The use of a single-bit quantizer ensures linearity (there are only two DAC levels and the $\Sigma\Delta$ “builds” the interpolation curve).
2. The quantization error is half of the full scale; therefore, there is a lot of noise around the loop.
3. The output of the integrators (op-amps) is made by signal and large noise.
4. The output dynamic range of the integrator must provide room for signal and much more for the noise.
5. Real integrators can saturate :(

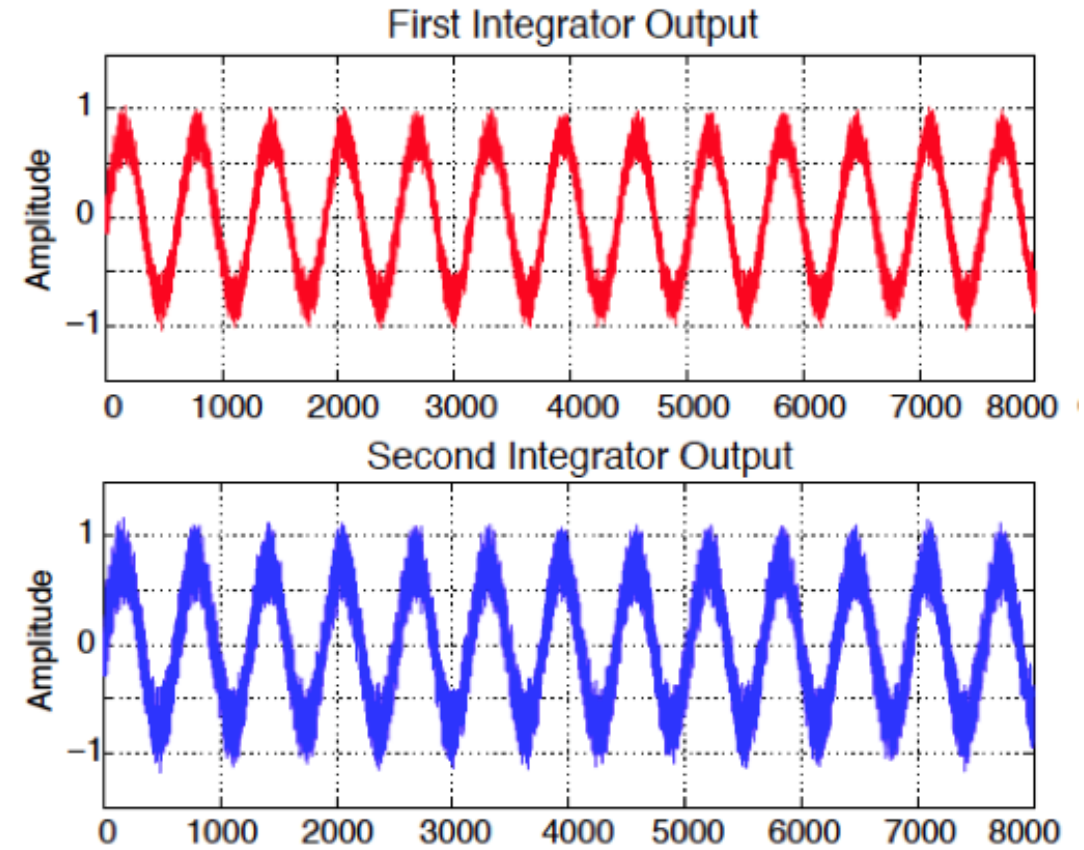


5.3 Sigma Delta and Incremental Converters

Single-bit Second Order

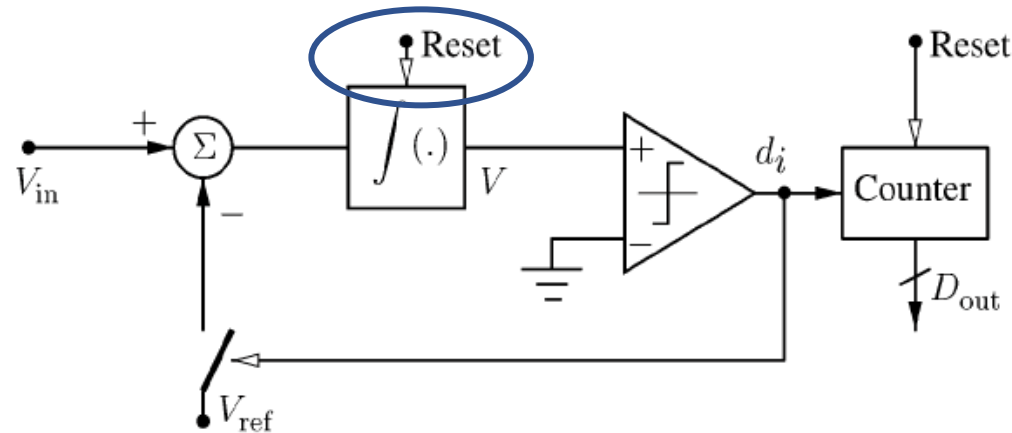


Multi-bit Second Order



5.3 Sigma Delta and Incremental Converters

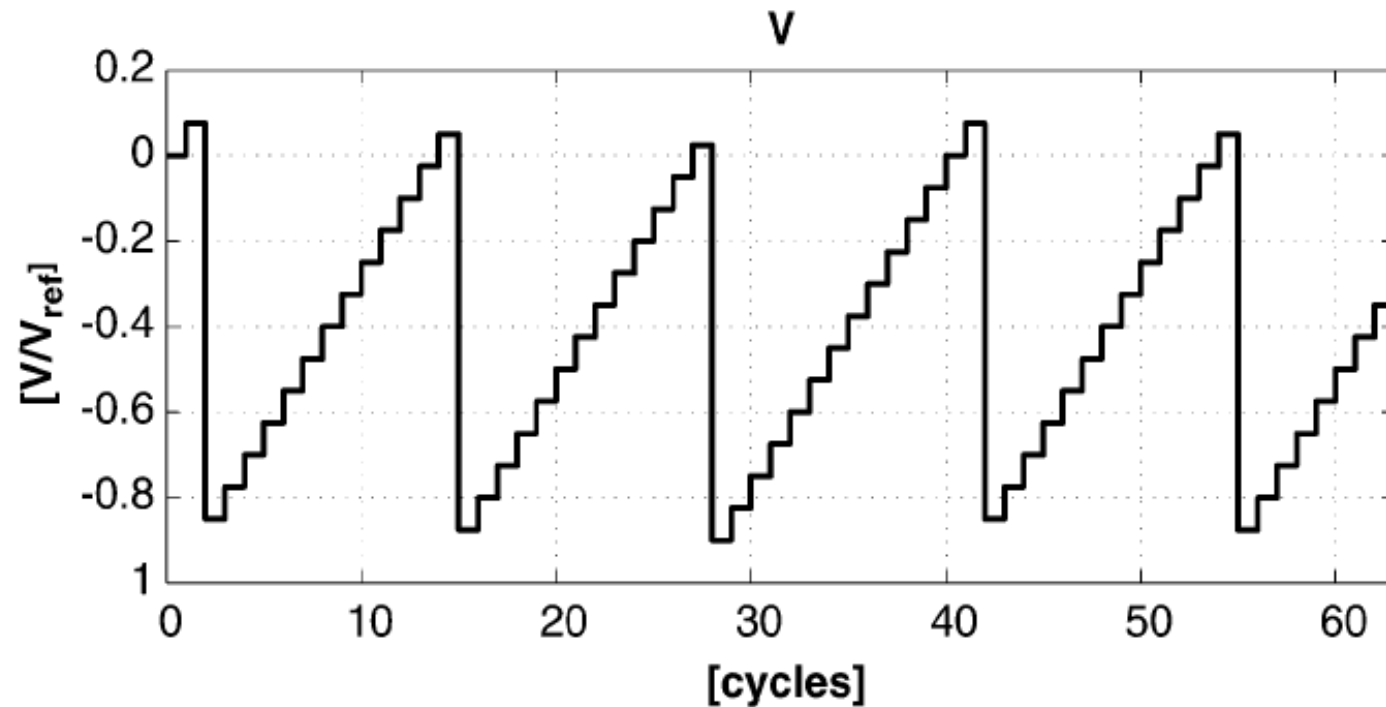
Incremental Converters



- ❑ Are Nyquist-rate converters.
- ❑ Are the modification and the extension of ramp converters. They use a cascade of integrators to accumulate many times the input signal (reset at the beginning).
- ❑ They use a DAC in feedback like Sigma-Delta
- ❑ Face stability and the use of the same architecture of a Sigma Delta is beneficial.
- ❑ Normally use a 1-bit DAC (to ensure linearity)
- ❑ Good for high resolution and low speed: need many clock periods for conversion.

5.3 Sigma Delta and Incremental Converters

First Order Op-Amp Output ($V_{in} = 0.075 V_{ref}$)



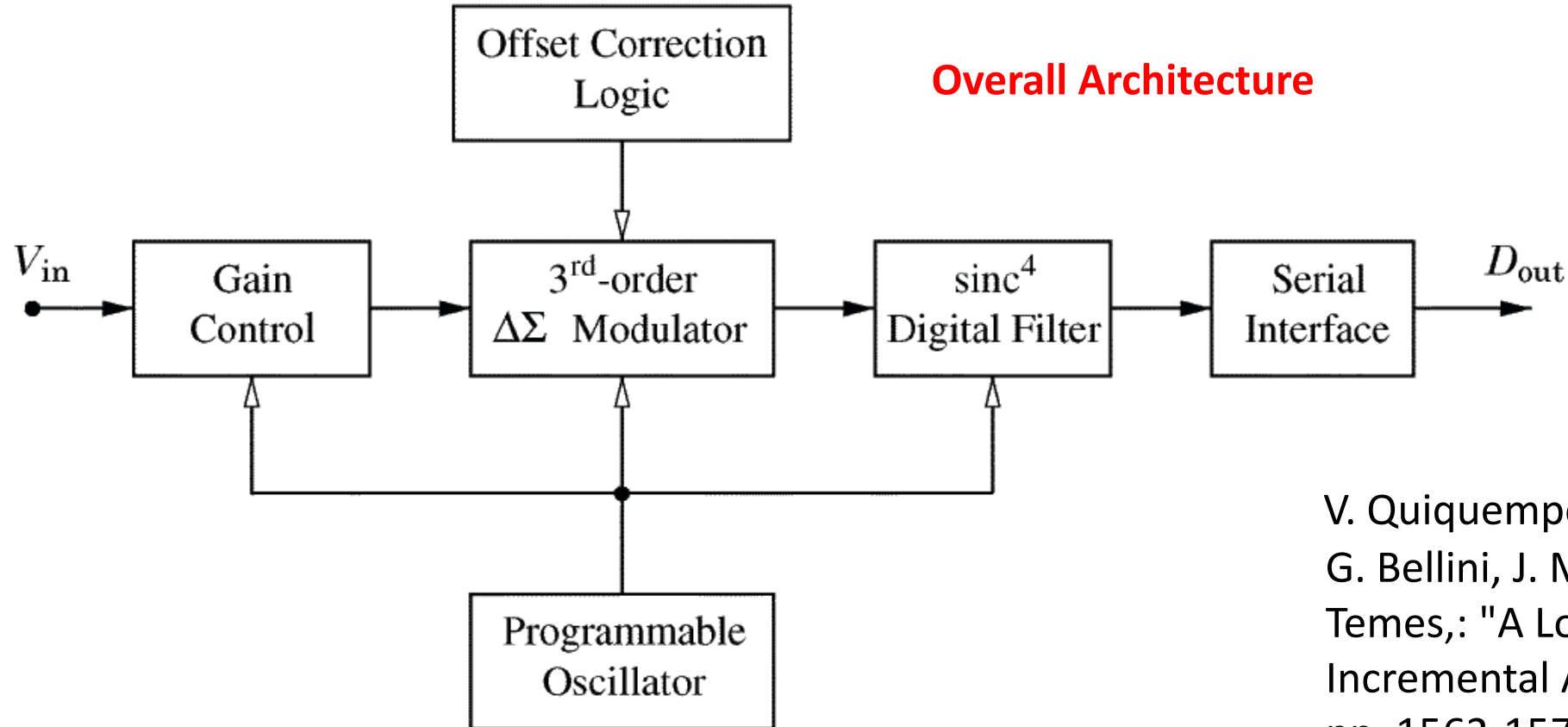
$$V = nV_{in} - NV_{ref}$$

$$N = n \left(\frac{V_{in}}{V_{ref}} \right) + \epsilon$$

5.3 Sigma Delta and Incremental Converters

DESIGN EXAMPLE

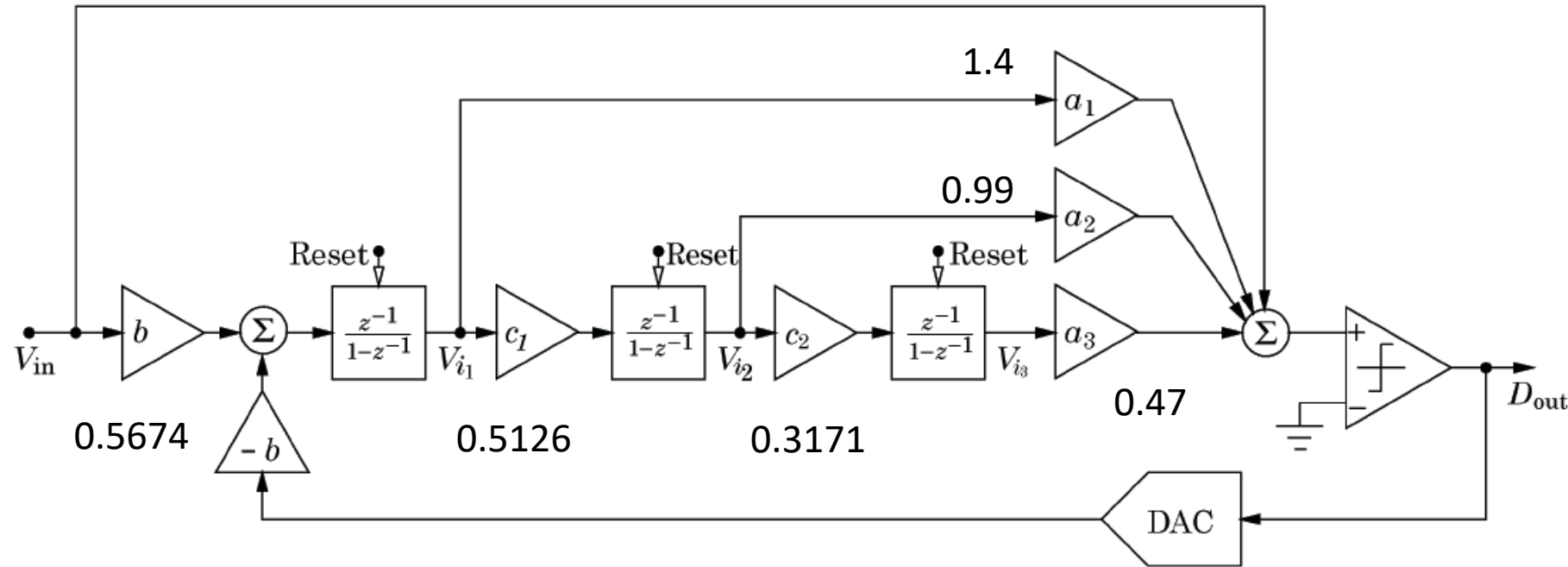
Overall Architecture



V. Quiquempoix, P. Deval, A. Barreto, G. Bellini, J. Márkus, J. Silva, and G. C. Temes, "A Low-Power 22-bit Incremental ADC"; IEEE JSSC. (2006), pp. 1562-1571.

5.3 Sigma Delta and Incremental Converters

Modulator Schematic



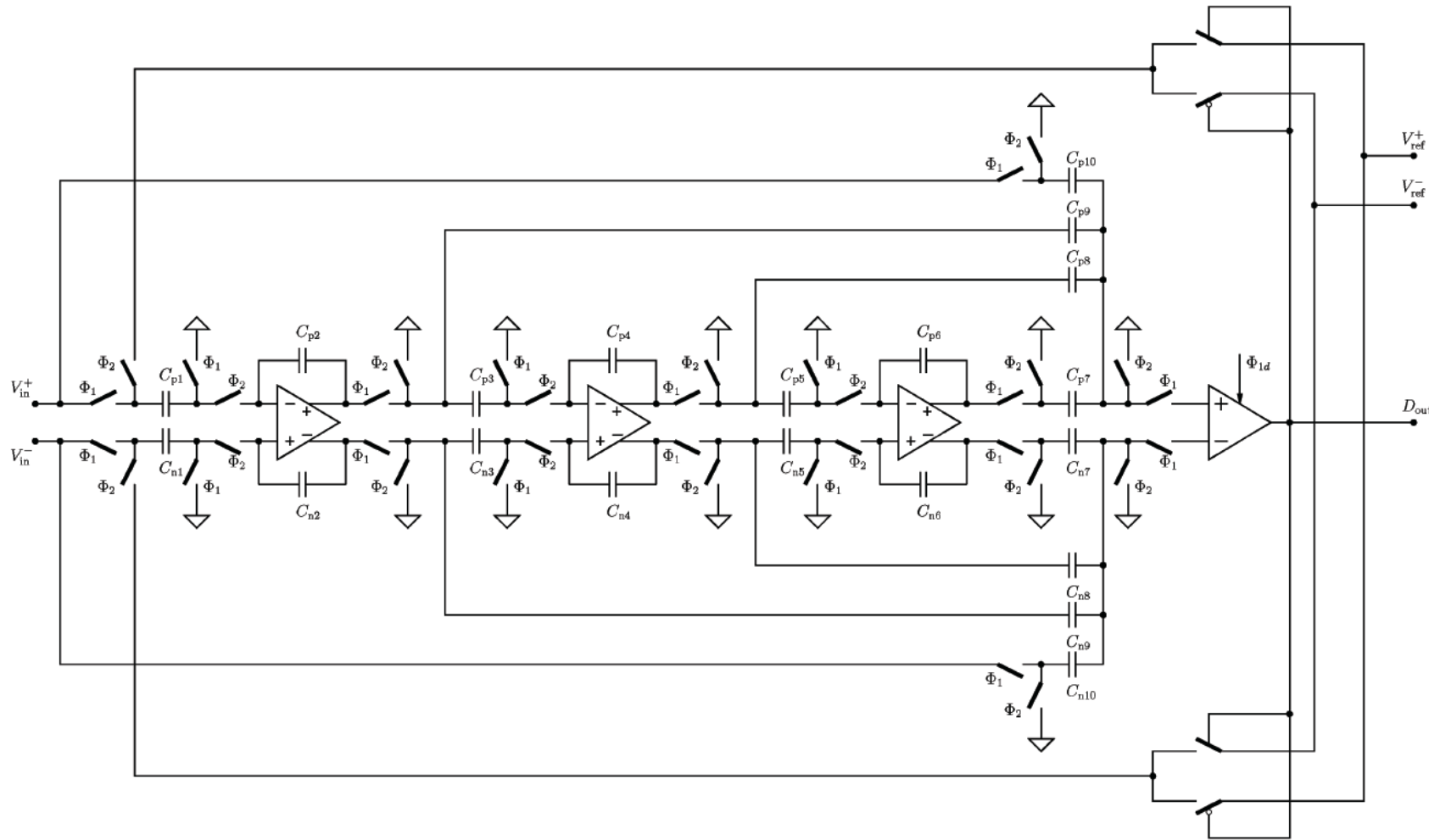
$$V_{i3}[n] = c_2 c_1 b \sum_{m=0}^{n-1} \sum_{l=0}^{m-1} \sum_{k=0}^{l-1} (V_{in}[k] - d_k V_{ref})$$

$$\frac{V_{in}}{V_{ref}} \approx \frac{3!}{(n-2)(n-1)n} \sum_{m=0}^{n-1} \sum_{l=0}^{m-1} \sum_{k=0}^{l-1} d_k$$

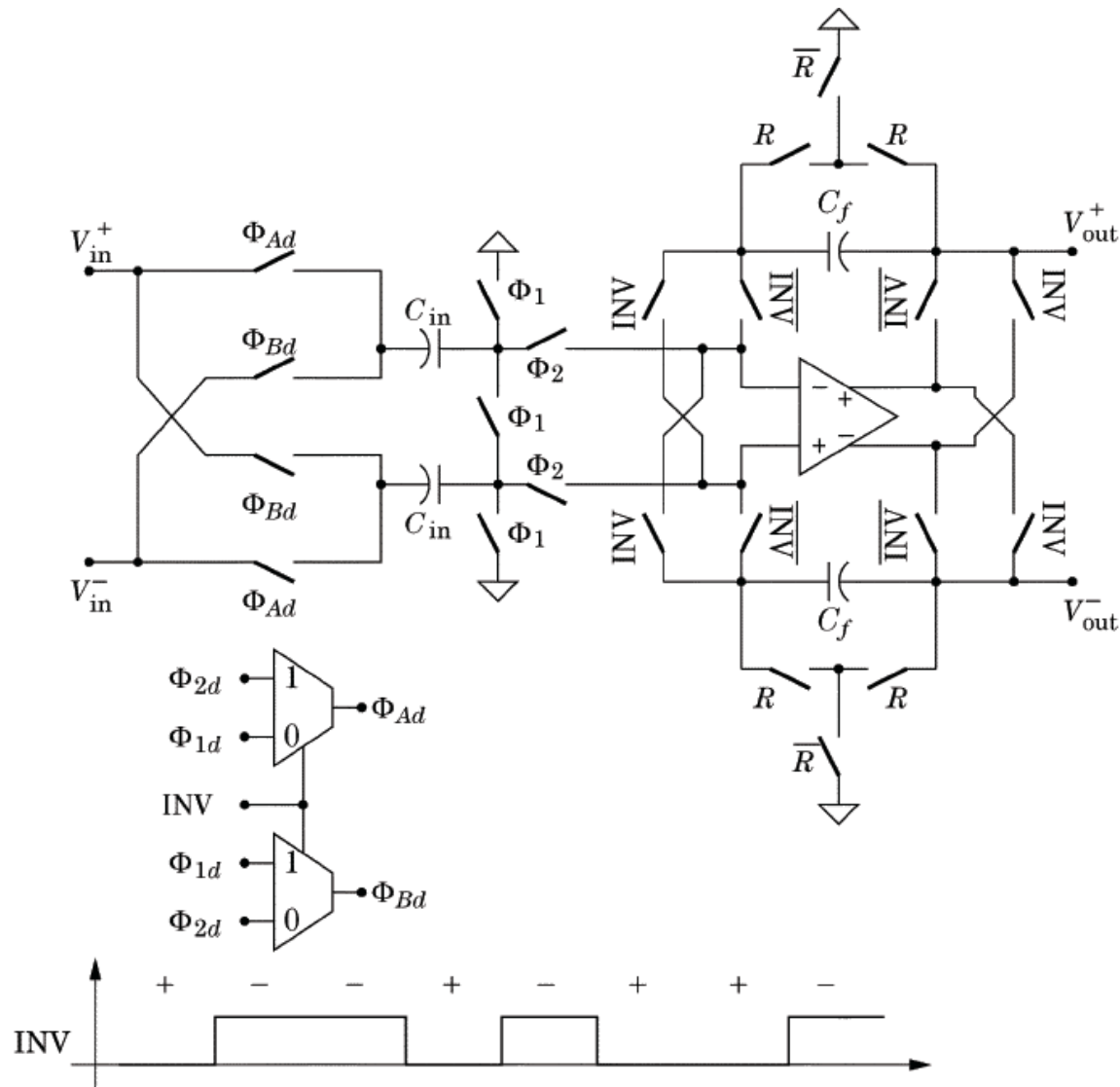
$$V_{LSB} \approx \frac{2 \cdot 3!}{(n-2)(n-1)n} \frac{1}{c_2 c_1 b} V_{ref}$$

5.3 Sigma Delta and Incremental Converters

Fully Differential Circuit



5.3 Sigma Delta and Incremental Converters



Offset Compensation

Fractal modulation

$+1, -1, +1, -1, \dots$

$((+-)(-+))$

$((+--+)(-++-))$

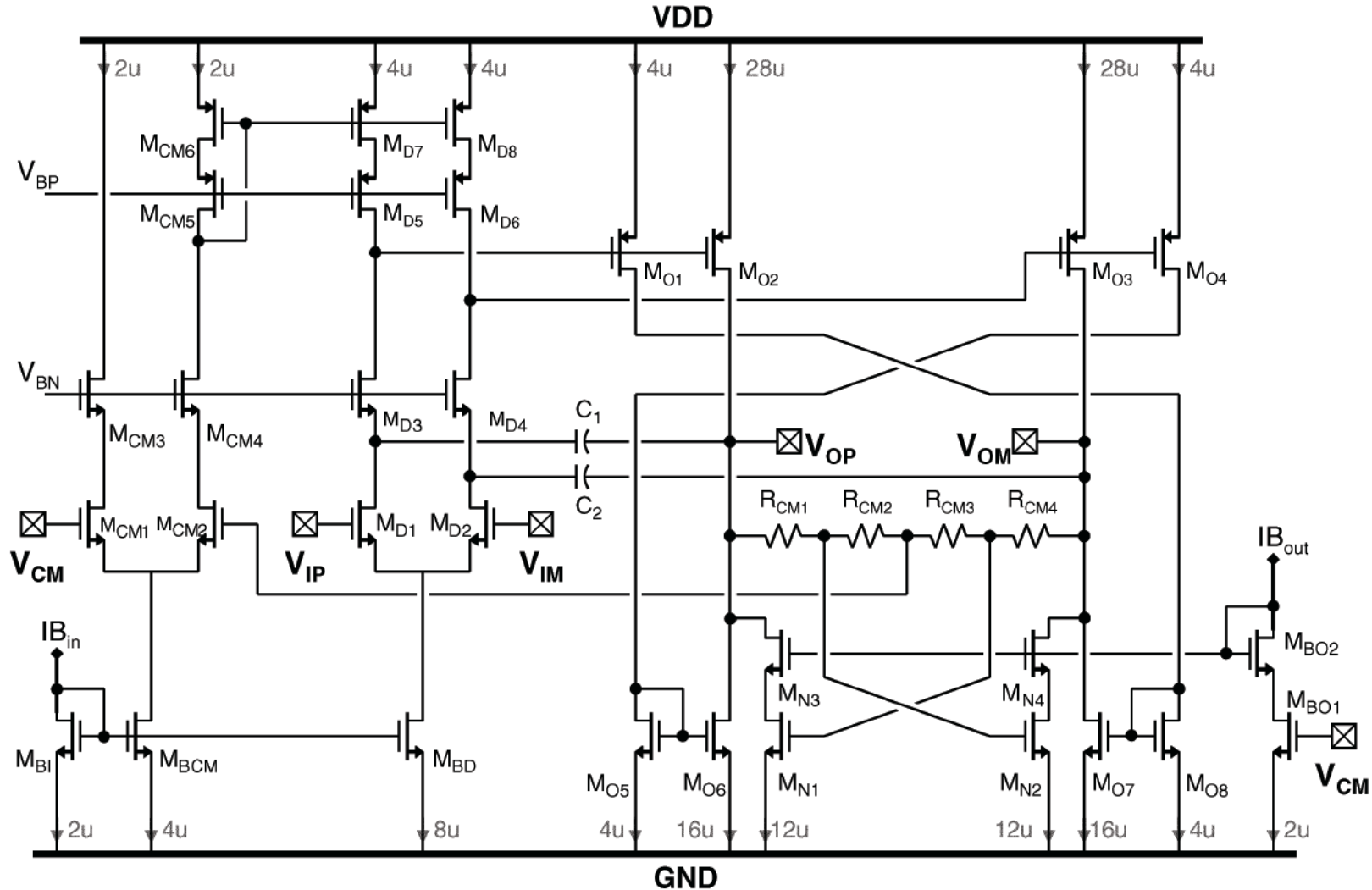
First Order

Second Order

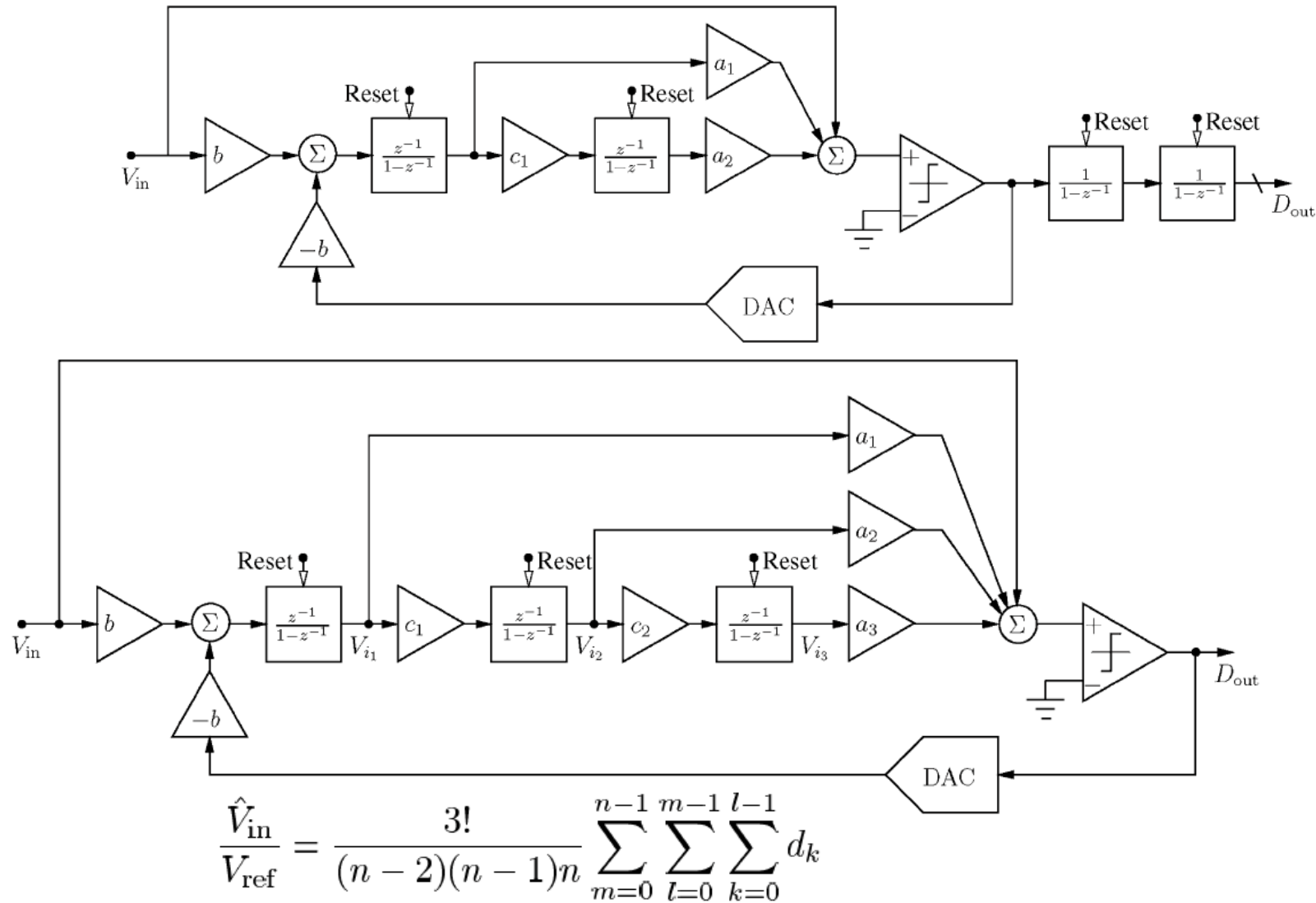
Third Order

5.3 Sigma Delta and Incremental Converters

Op-Amp Schematic

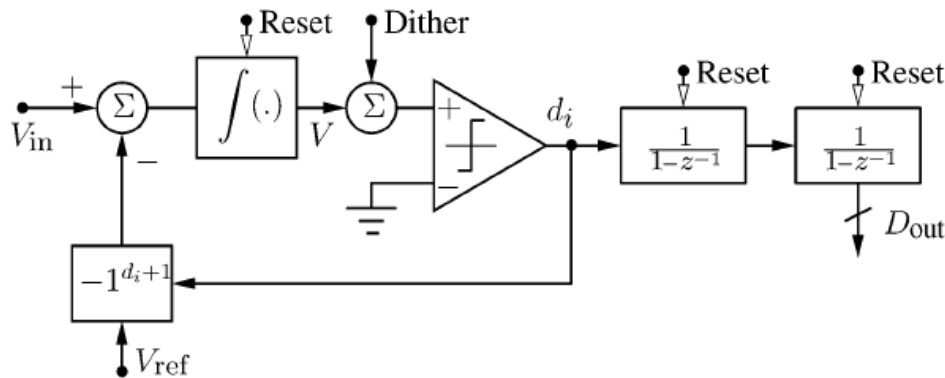


5.3 Sigma Delta and Incremental Converters



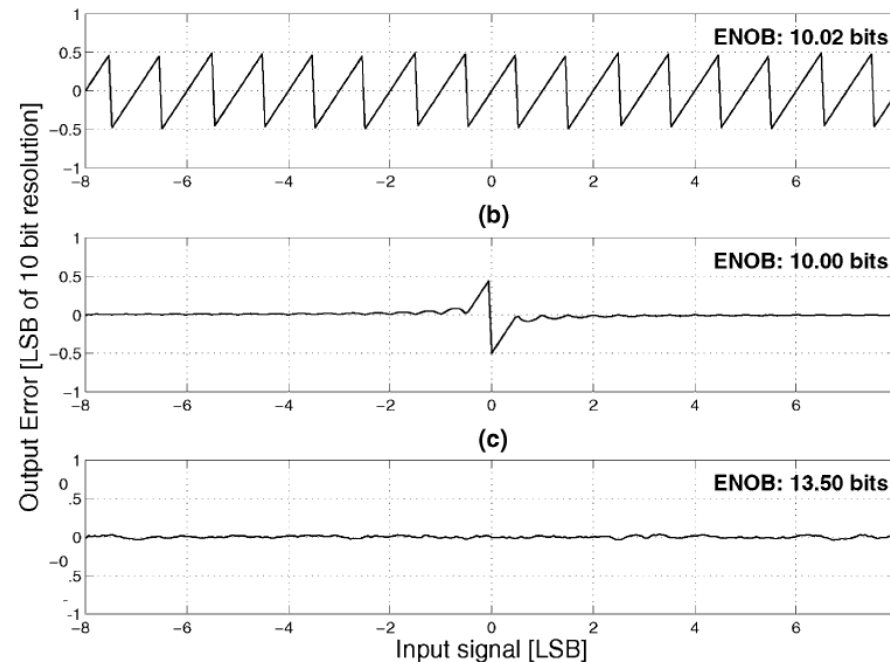
5.3 Sigma Delta and Incremental Converters

- Sigma-delta use sinc^n filters
- Incremental don't handle shaped noi
- Same digital processing of input
or
- Use an extra accumulator



COMPARISON OF FIRST-ORDER INCREMENTAL CONVERTERS II

Type of Digital Filter	Resolution (Accuracy)	Number of Cycles
second-order sinc	8.6 bit	1024
1 integrator (counter)	10.0 bit	1024
second-order sinc with dither	12.2 bit	1024
2 integrators with dither	13.5 bit	1024



5.3 Sigma Delta and Incremental Converters

Second Order

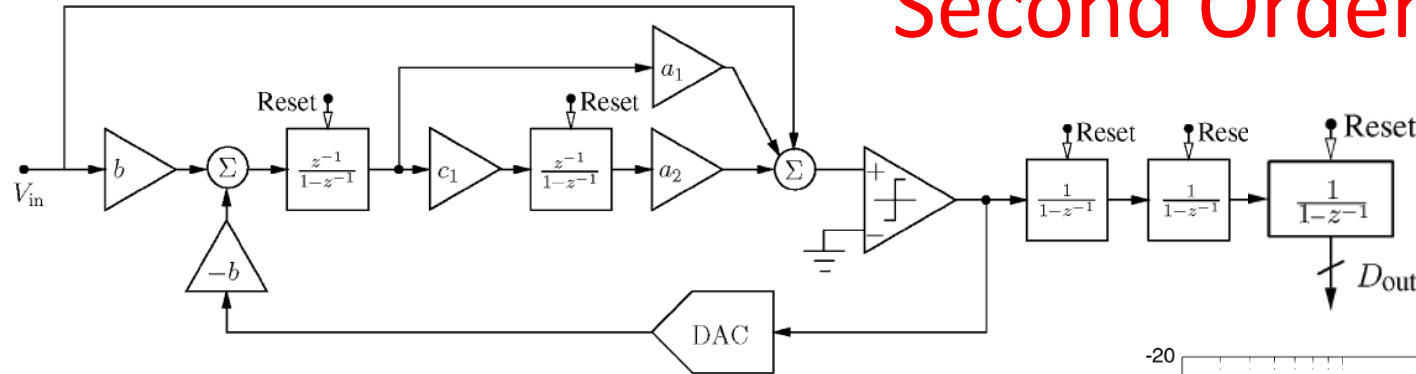
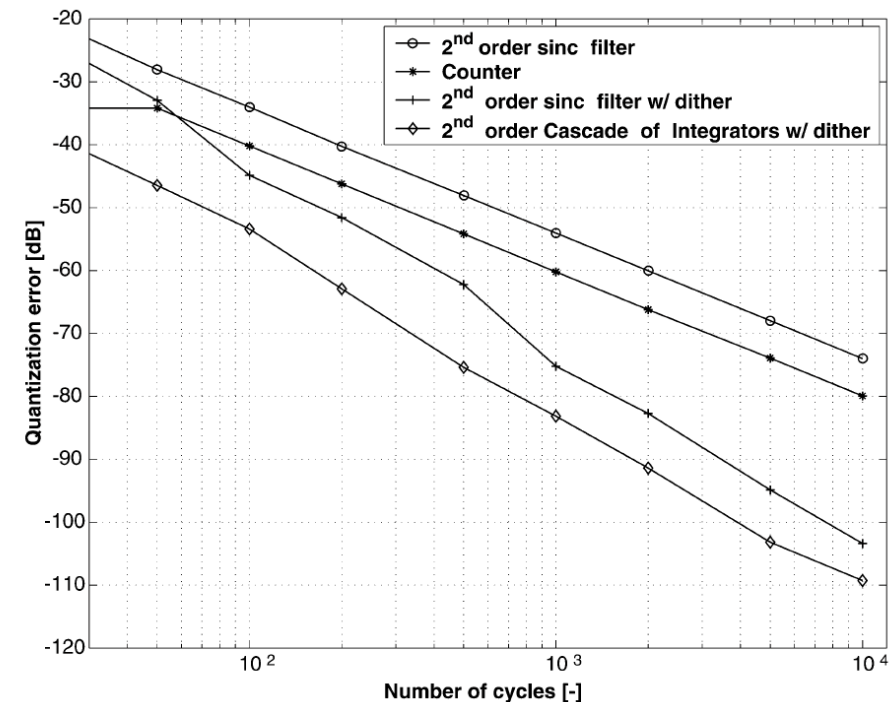


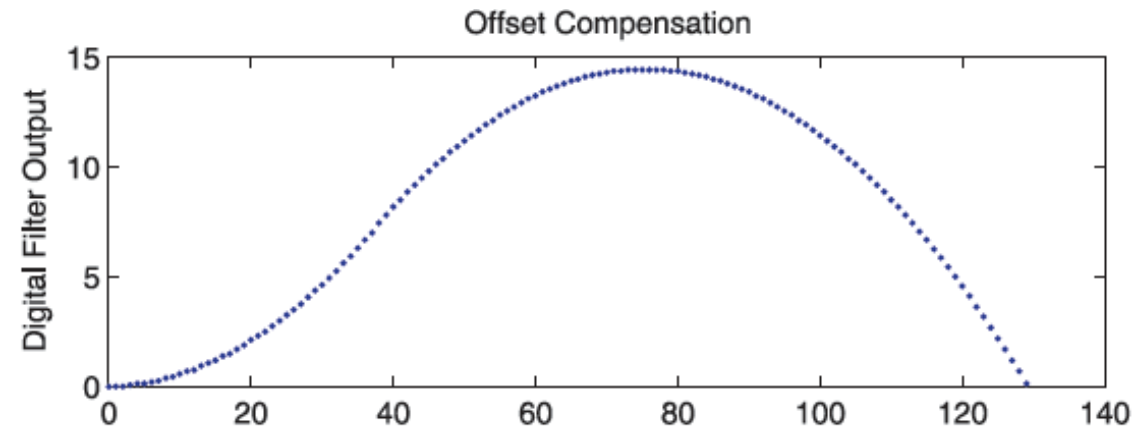
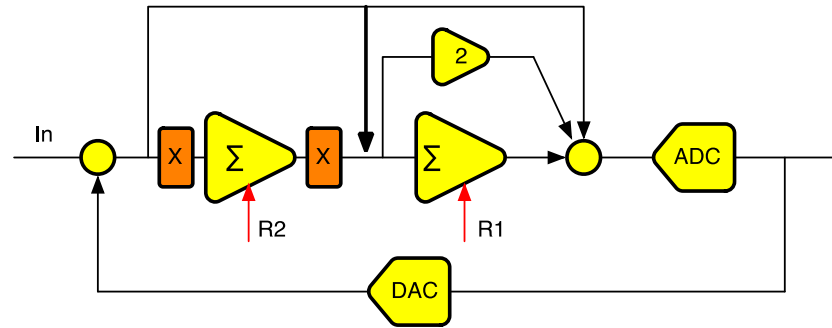
TABLE IV
COMPARISON OF HIGHER ORDER INCREMENTAL CONVERTERS

Order of Modulator	Type of Digital Filter	Resolution (Accuracy)	Total Number of Cycles
2	2 integrators	16	537
2	2 integrators [†]	16	381
2	second-order sinc	16	1092
2	third-order sinc	16	576
3	3 integrators	16	158
3	3 integrators [†]	16	127
3	fourth-order sinc	16	350



5.3 Sigma Delta and Incremental Converters

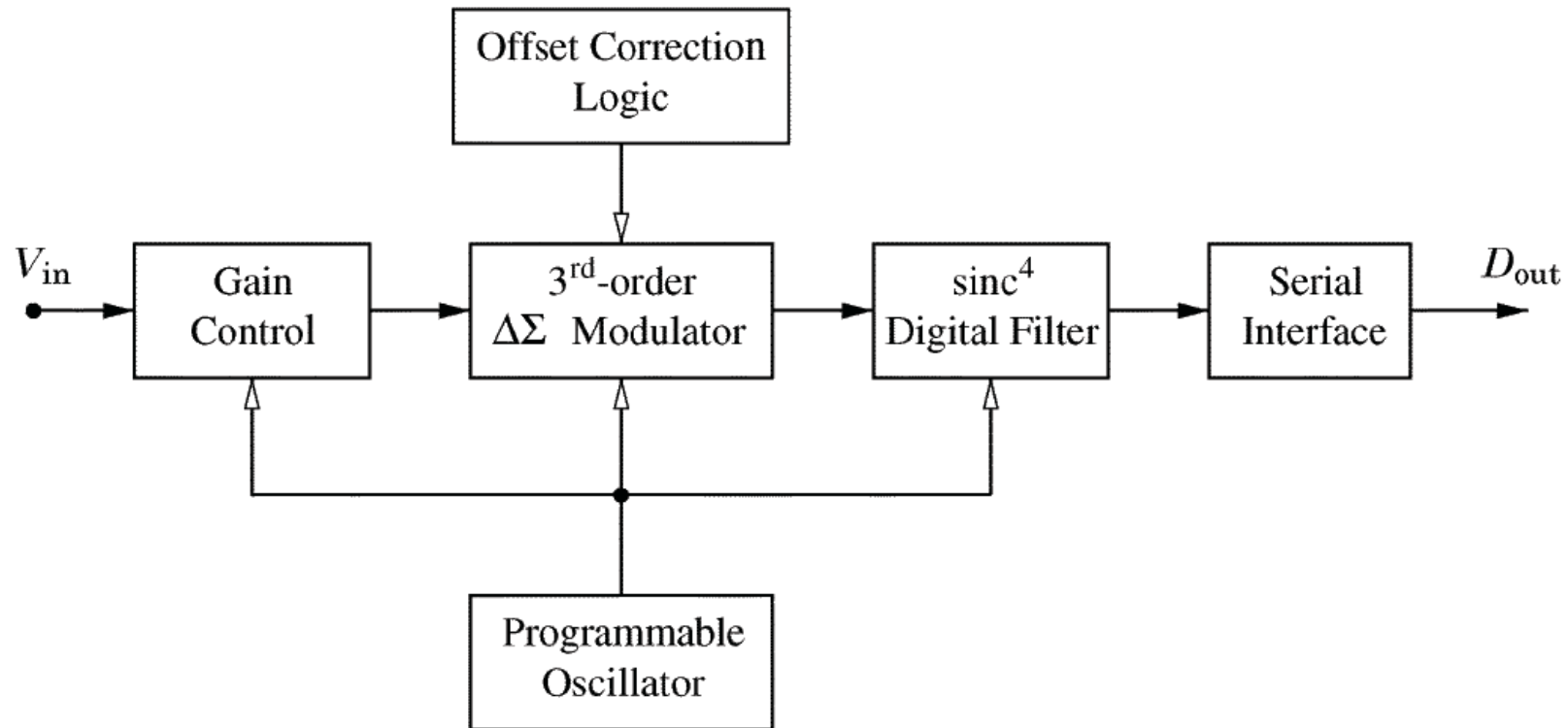
One step
chopping



5.3 Sigma Delta and Incremental Converters

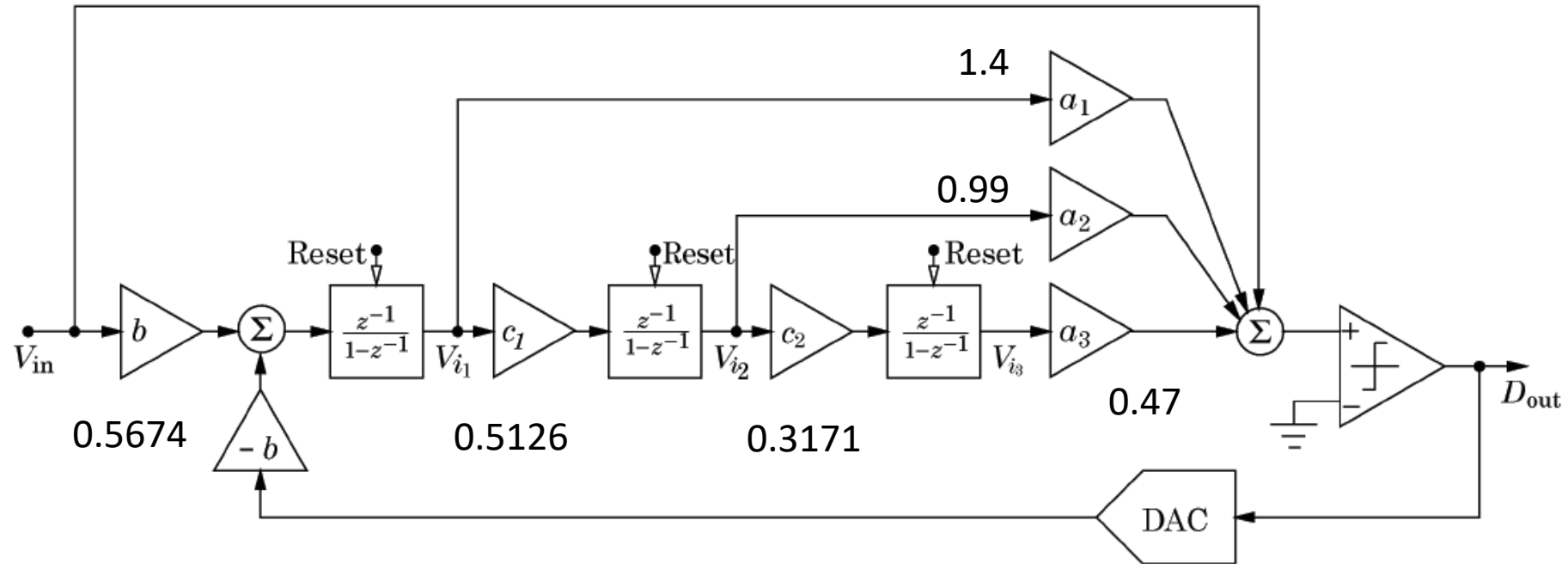
V. Quiquempoix, P. Deval, A. Barreto, G. Bellini, J. Márkus,
J. Silva, and G. C. Temes,: "A Low-Power 22-bit Incremental ADC"; IEEE JSSC. (2006), pp. 1562-1571

Overall Architecture



5.3 Sigma Delta and Incremental Converters

Modulator Schematic



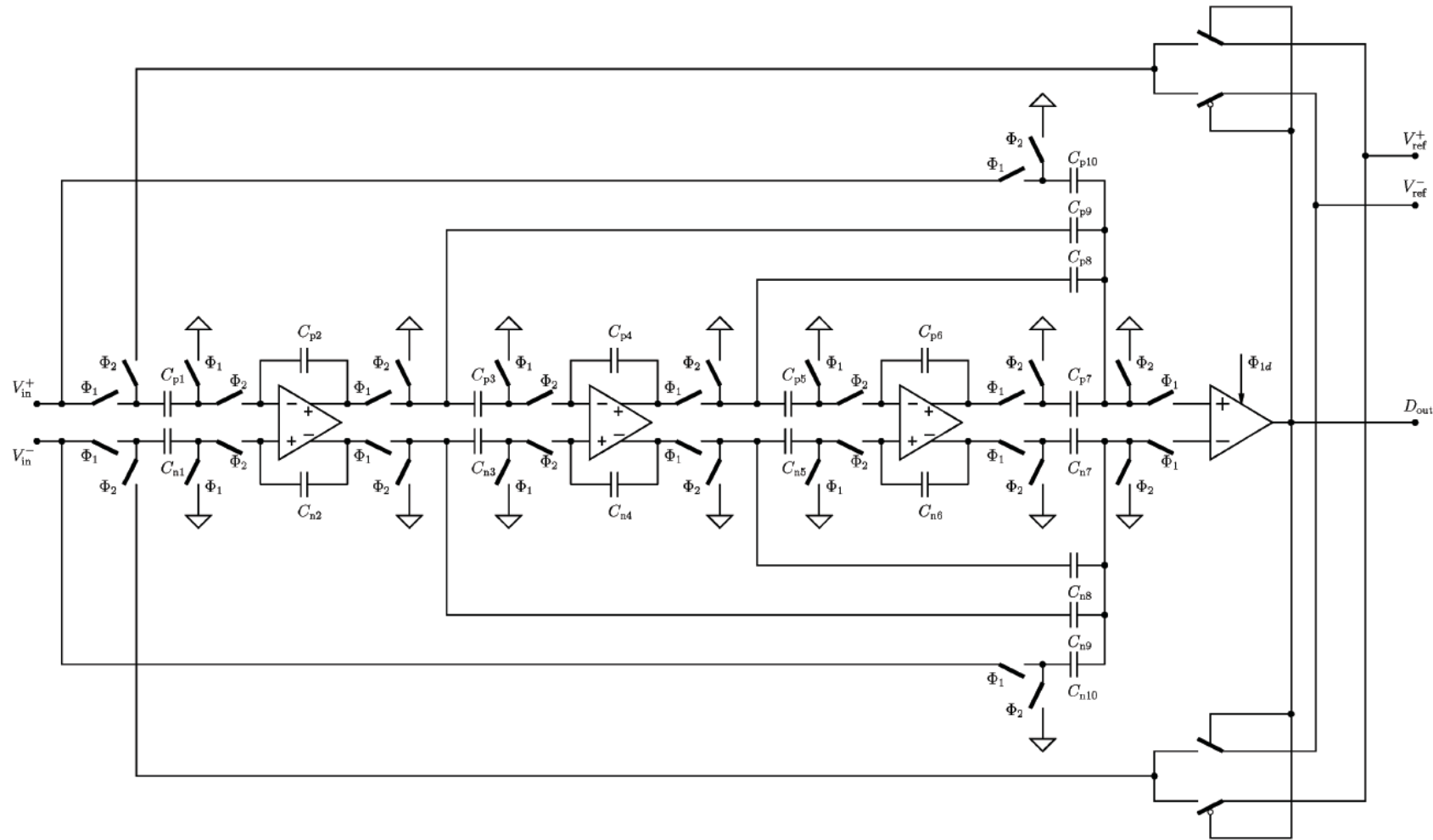
$$V_{i3}[n] = c_2 c_1 b \sum_{m=0}^{n-1} \sum_{l=0}^{m-1} \sum_{k=0}^{l-1} (V_{in}[k] - d_k V_{ref})$$

$$\frac{V_{in}}{V_{ref}} \approx \frac{3!}{(n-2)(n-1)n} \sum_{m=0}^{n-1} \sum_{l=0}^{m-1} \sum_{k=0}^{l-1} d_k$$

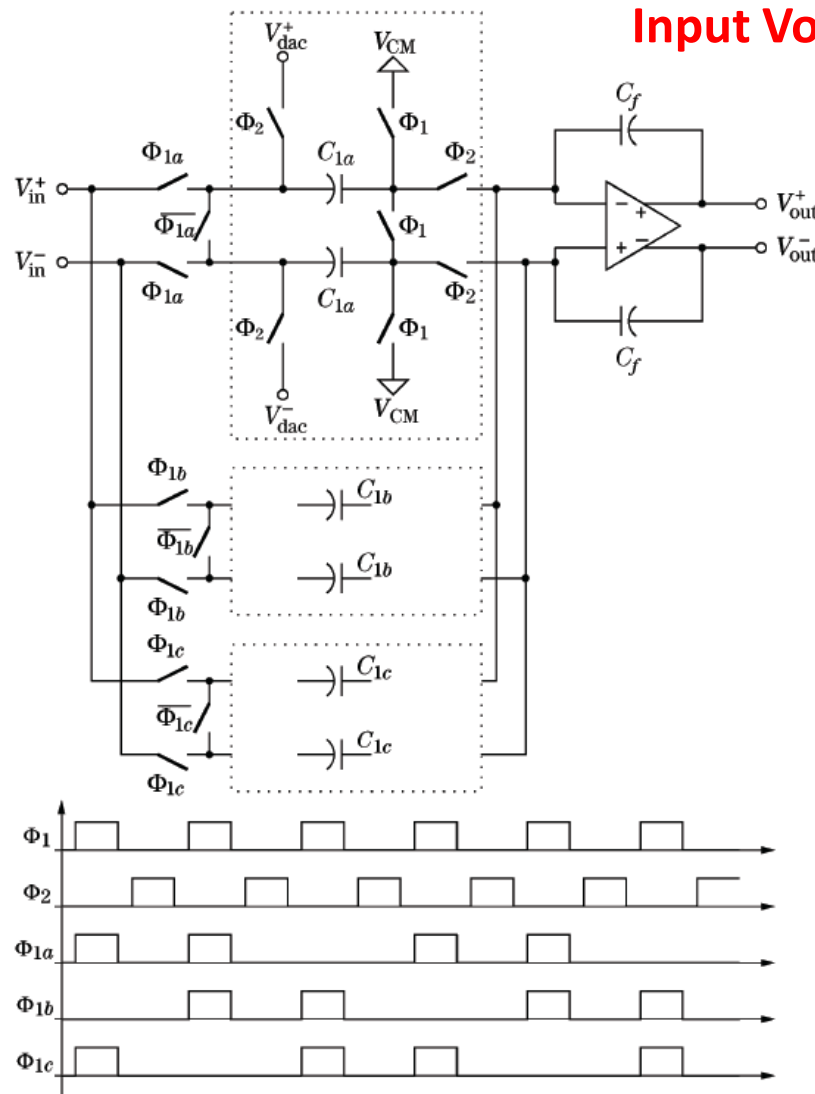
$$V_{LSB} \approx \frac{2 \cdot 3!}{(n-2)(n-1)n} \frac{1}{c_2 c_1 b} V_{ref}$$

5.3 Sigma Delta and Incremental Converters

Fully Differential Circuit



5.3 Sigma Delta and Incremental Converters



Input Voltage Attenuation

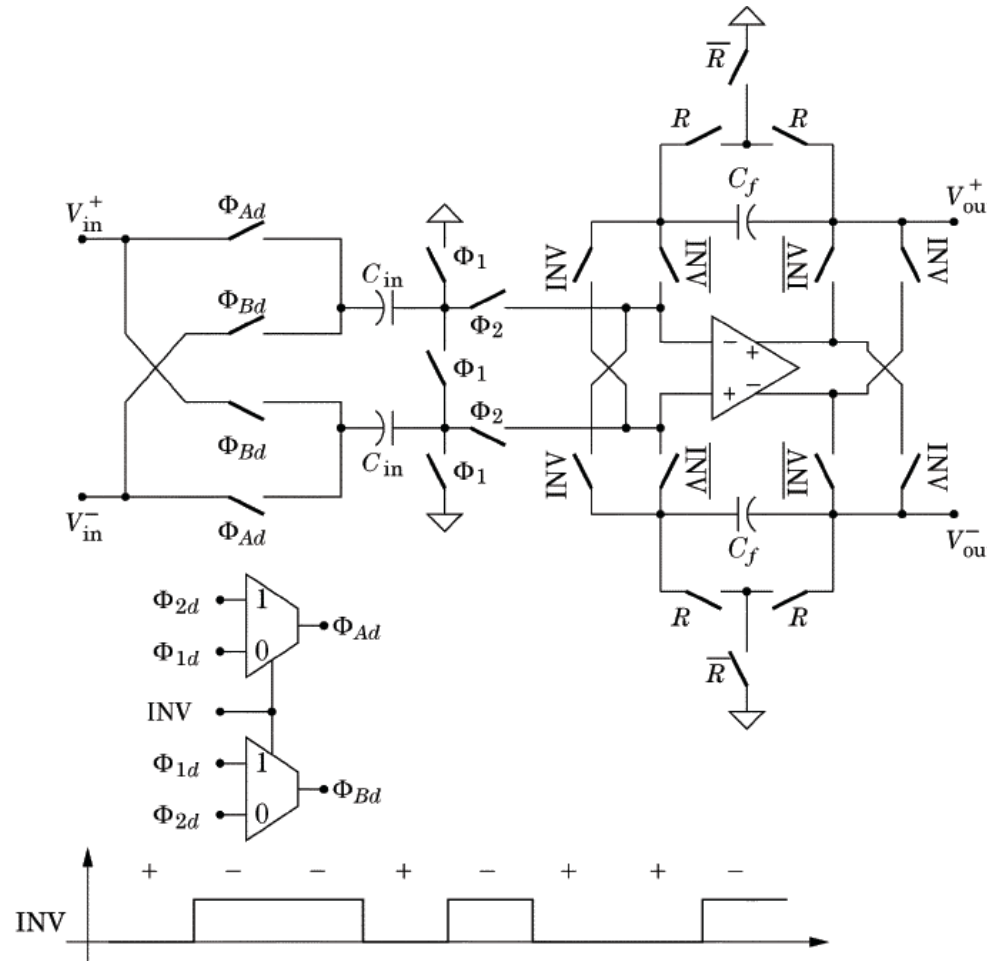
Full scale input causes overloading

Use of a circuit that injects 3 times the reference and two times the input signal

$$Q_{in} = C_{in} \left(\frac{2}{3} V_{in} - V_{dac} \right)$$

5.3 Sigma Delta and Incremental Converters

Offset Compensation



Fractal modulation

$+1, -1, +1, -1, \dots$

$((+-)(-+))$

$((+--+)(-++-))$

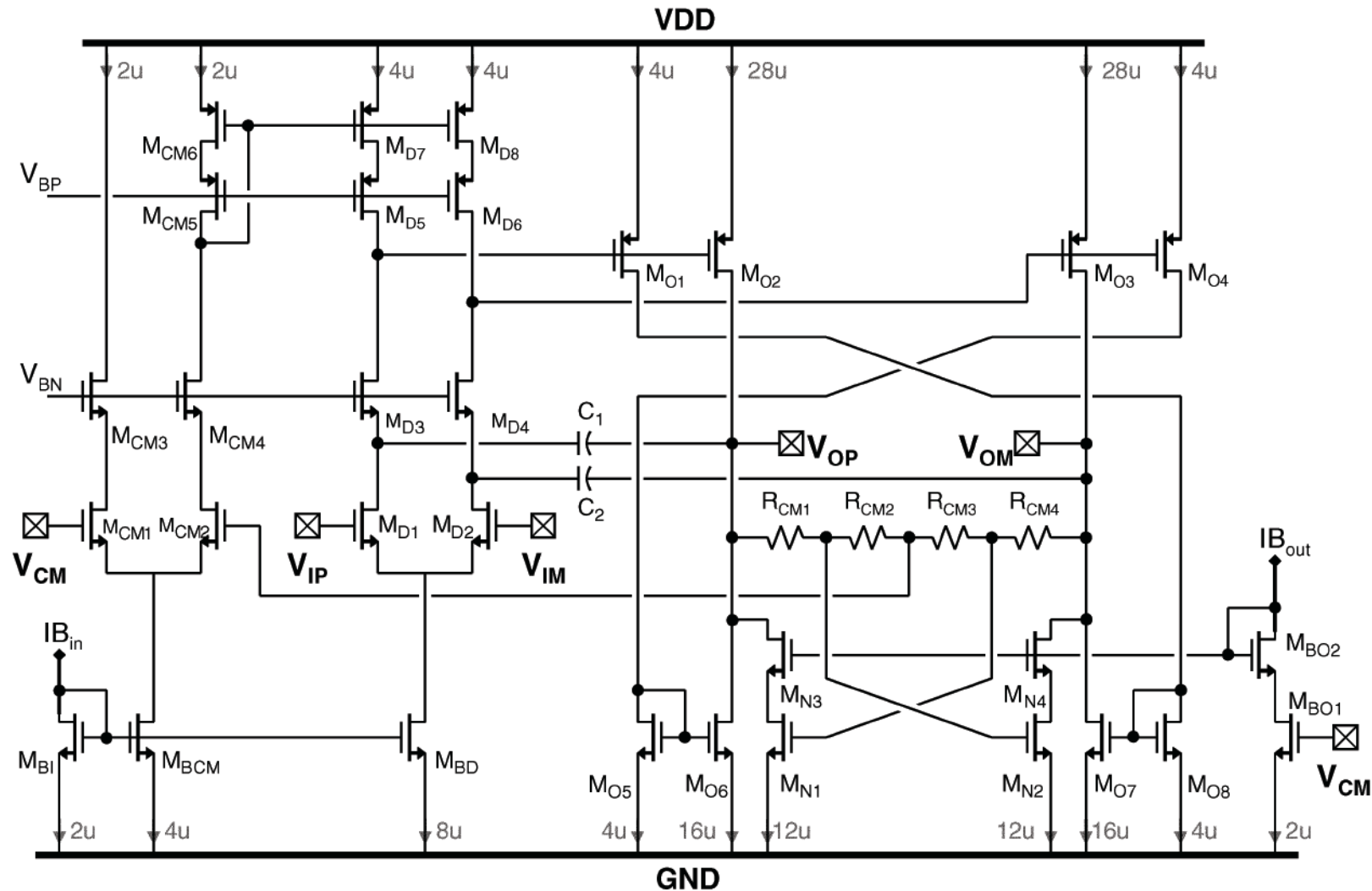
First Order

Second Order

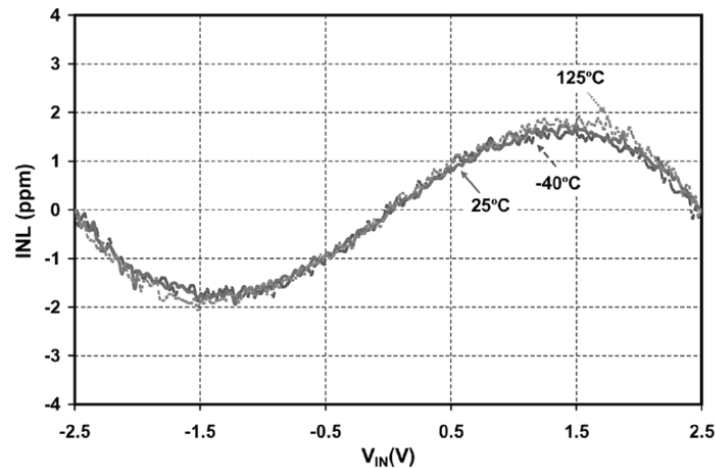
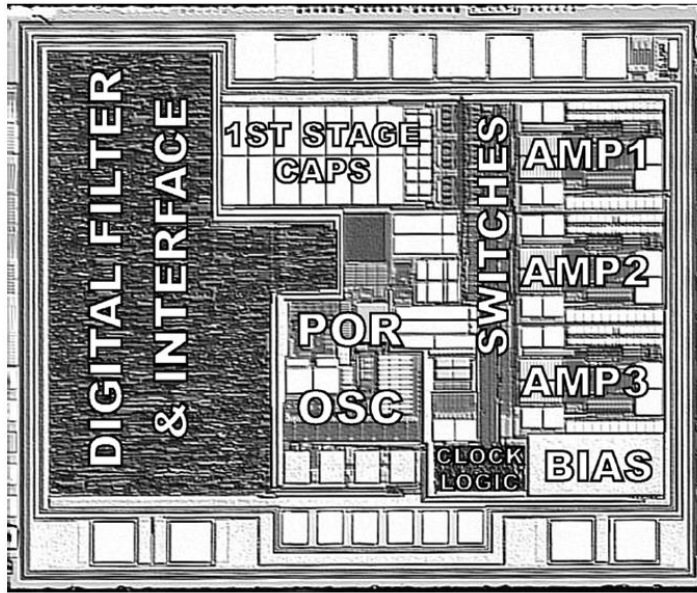
Third Order

5.3 Sigma Delta and Incremental Converters

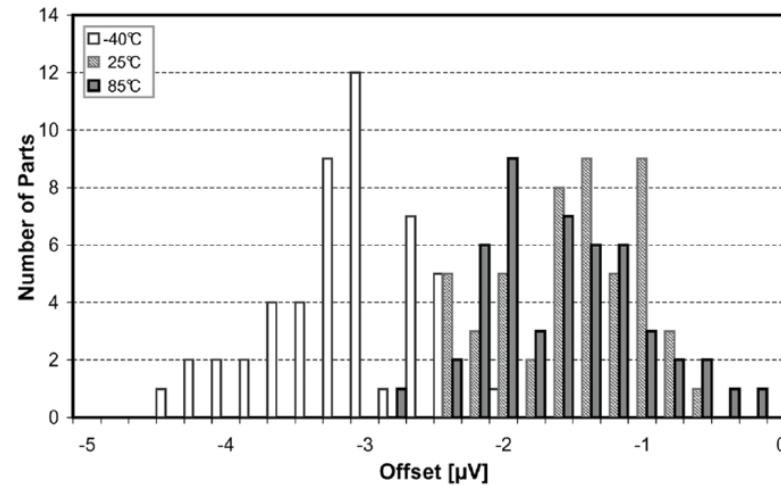
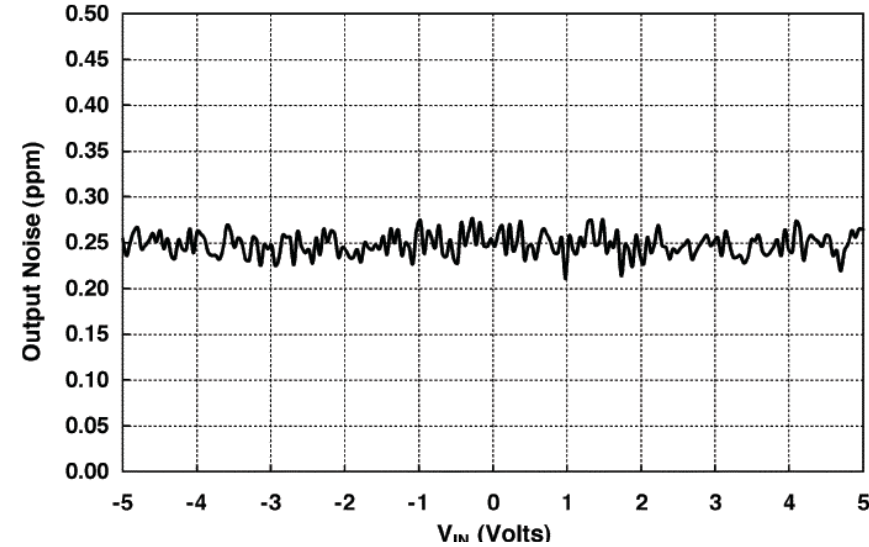
Op-Amp Schematic



5.3 Sigma Delta and Incremental Converters



Measurements

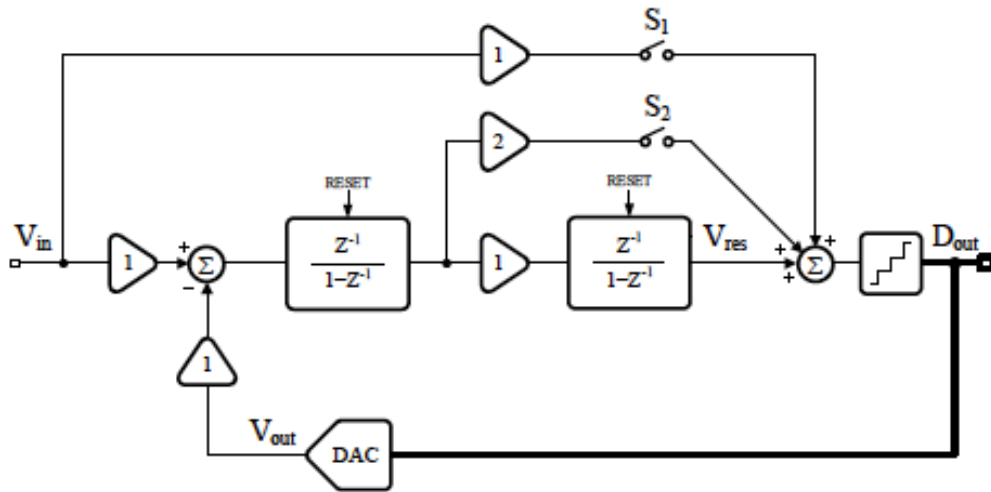


5.3 Sigma Delta and Incremental Converters

SUMMARY OF THE MEASURED PERFORMANCE OF THE INCREMENTAL ADC

Parameter	Performance
Conversion time	
typ.	66.7 ms
DC offset	
typ.	2 μV (1.7 LSB)
max.	10 μV (8.4 LSB)
Gain Error [†]	
typ.	2 ppm (8 LSB)
max.	10 ppm (40 LSB)
INL [†]	
$V_{\text{ref}} = 2.5 \text{ V}$	max. 4 ppm (16 LSB)
$V_{\text{ref}} = 5 \text{ V}$	max. 10 ppm (40 LSB)
Supply Current	
Shutdown mode	max. 1 μA
Op. mode $V_{\text{DD}} = 5 \text{ V}$	typ. 120 μA
Op. mode $V_{\text{DD}} = 3 \text{ V}$	typ. 100 μA
CMRR [‡] @ 50/60 Hz	at least 135 dB
DC PSRR [‡]	
$V_{\text{DD}} = 2.5 \sim 6 \text{ V}$	at least 120 dB
Output Noise [†]	
$V_{\text{ref}} = 5 \text{ V}$	0.25 ppm (2.5 μV_{RMS} , or 1 LSB)
$V_{\text{ref}} = 2.5 \text{ V}$	0.48 ppm (2.4 μV_{RMS} , or 2 LSB)

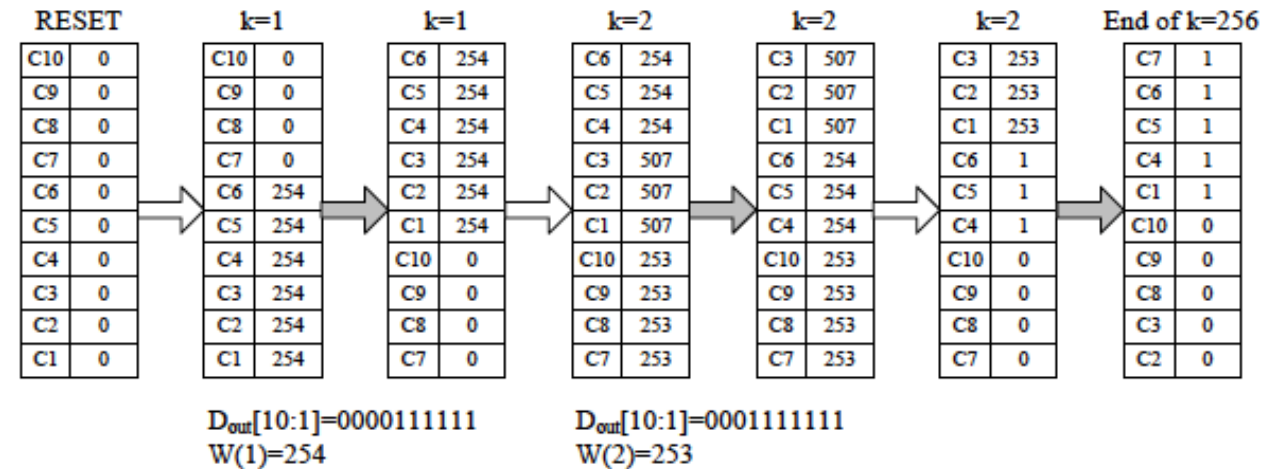
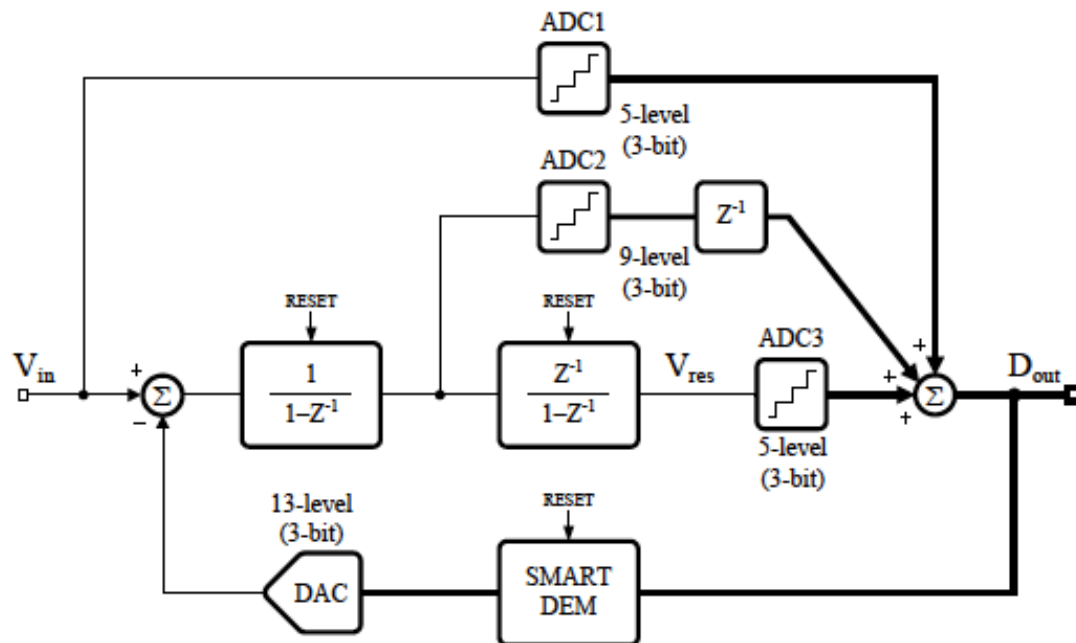
5.3 Sigma Delta and Incremental Converters



Avoiding the analog summing node

Use of smart DEM for multi-bit operation

The idea of Smart-DEM algorithm is to dynamically balance the weights of error along the data conversion of N clock periods for one sample.



Y. Liu, E. Bonizzoni, A. D'Amato, and F. Maloberti, "A 105-dB SNDR, 10 kSps Multi-Level Second-Order Incremental Converter with Smart-DEM Consuming 280 uW and 3.3-V Supply", IEEE ESSCIRC, 2013, pp. 371-374.

5.3 Sigma Delta and Incremental Converters

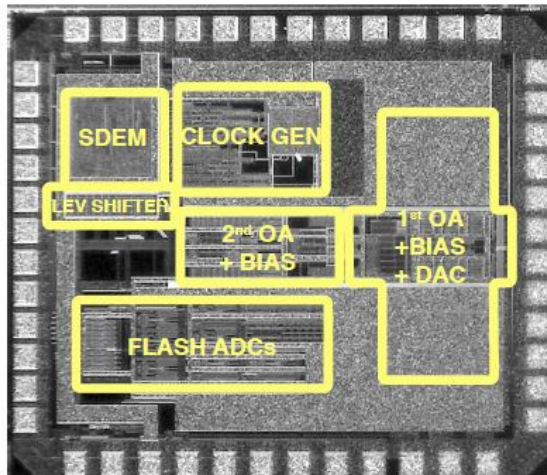
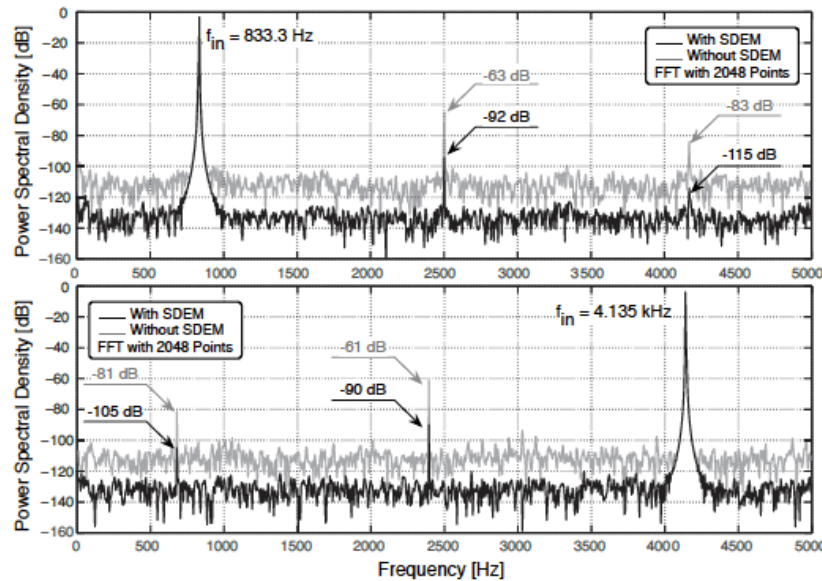


Table 2 Performance Comparison between proposed incremental ADC with state of the art.

	This Work	ISSCC2013 [7]	ISSCC2013 [8]	ANALOG INTEGR CIRC S.[4]	JSSC2010 [9]	JSSC2005 [3]
Year	2013	2013	2013	2012	2010	2006
BW (Hz)	$5 \cdot 10^3$	12.5	667	$1 \cdot 10^3$	$500 \cdot 10^3$	7.5
F_S (Hz)	$10 \cdot 10^3$	25	$1.333 \cdot 10^3$	$2 \cdot 10^3$	$1 \cdot 10^6$	15
SNDR (dB)	105	119.8	81.9	110.7	86.3	123
Power (mW)	0.28	$6.3 \cdot 10^{-3}$	$19.9 \cdot 10^{-3}$	6	38.1	0.6
V_{DD} (V)	3.3	1.8	1.0	3.3	1.8	2.7-5.0
Technology (μm)	0.5-0.18	0.16	0.16	0.6-0.18	0.18	0.6
FOM _W (fJ/conv-step)	260	314.8	1475.7	5722	1460	9537
FOM _S (dB)	174.9	182.7	157.1	162.8	160.3	166.4

Y. Liu, E. Bonizzoni, A. D'Amato, and F. Maloberti, "A 105-dB SNDR, 10 kSps Multi-Level Second-Order Incremental Converter with Smart-DEM Consuming 280 μW and 3.3-V Supply", IEEE ESSCIRC, 2013, pp. 371-374.

6. Low Voltage Low Power Circuits

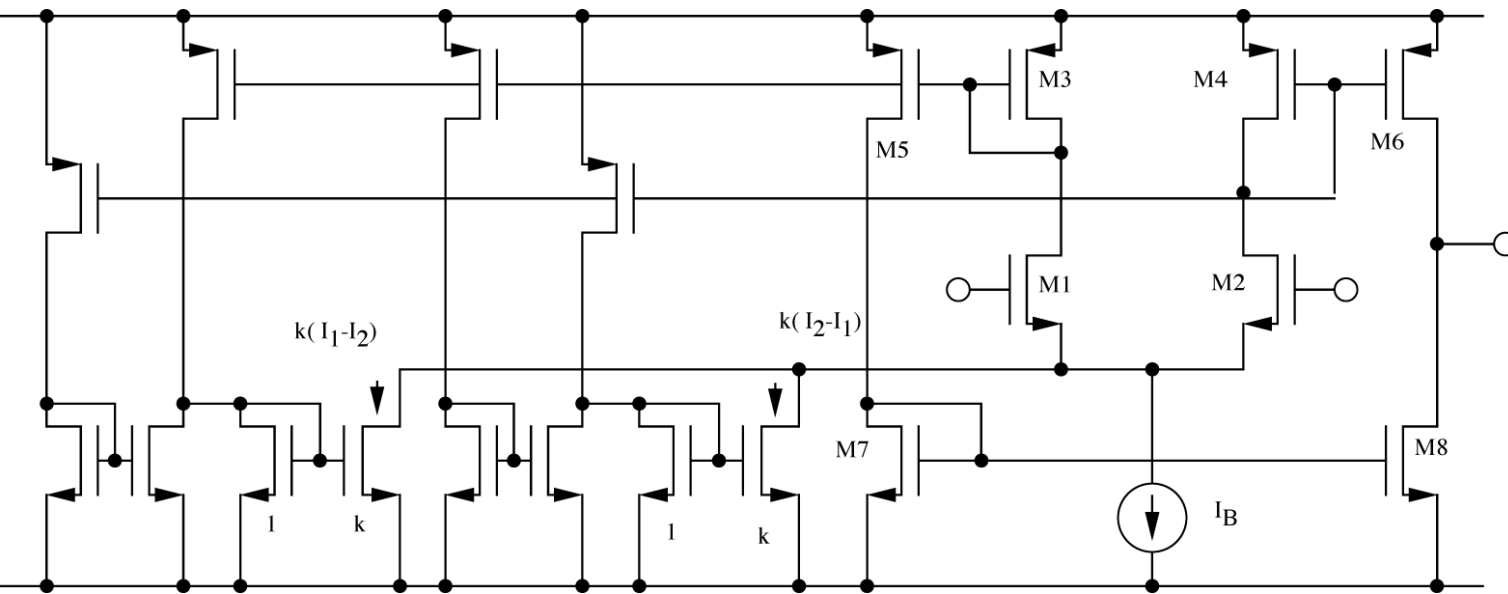
Content

- 6.1 Low Voltage Low Power Analog Cells
- 6.2 Low Voltage Reference Generator

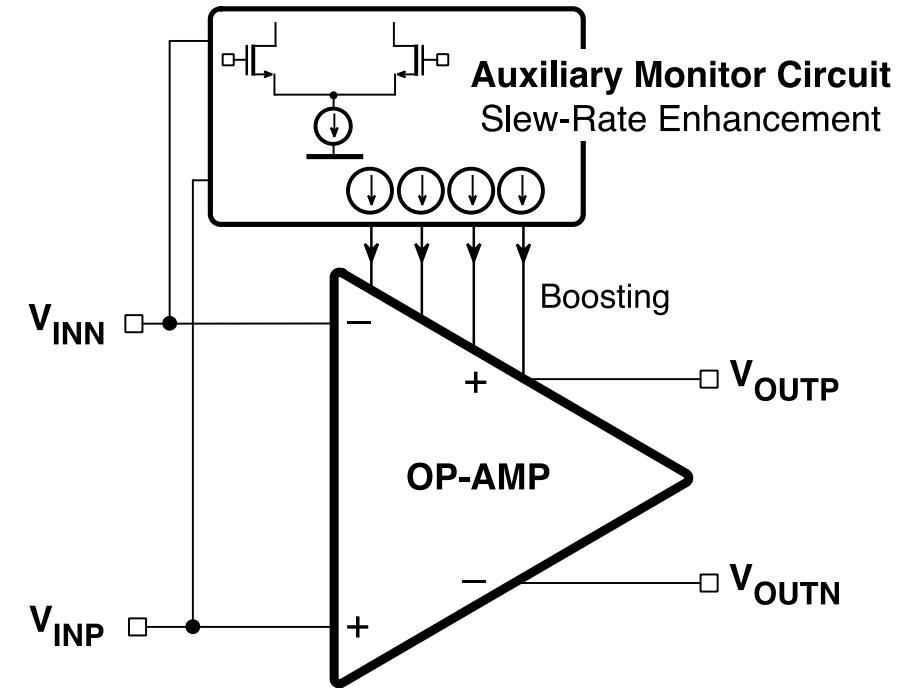
6.1 Low Voltage Low Power Analog Cells

Op-amp with very low bias current suffer from a low SR

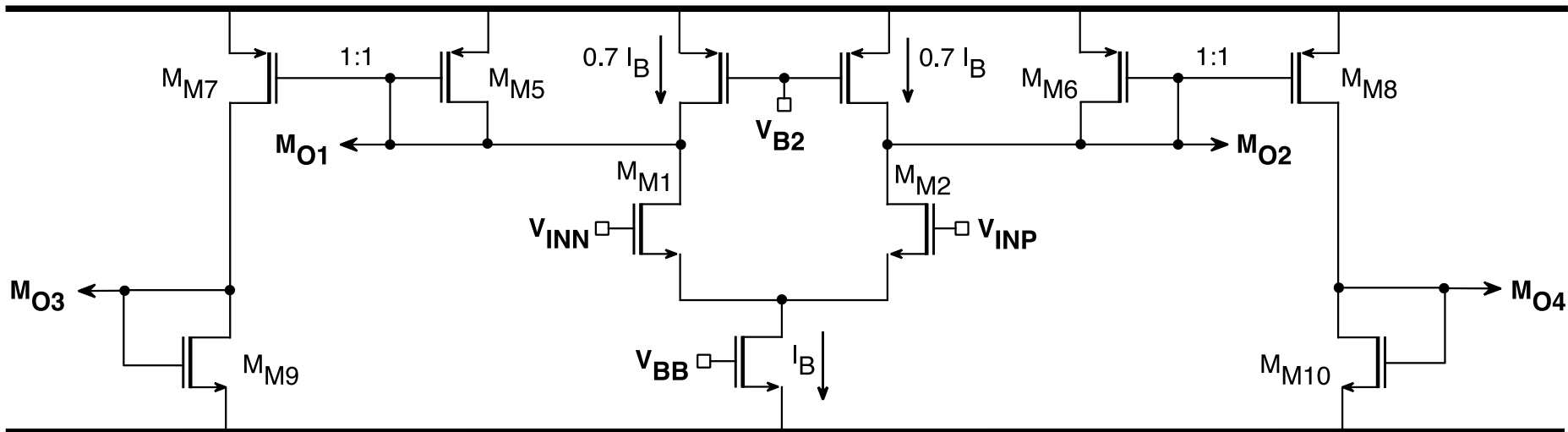
Dynamic biasing of the tail current (E. Vittoz)



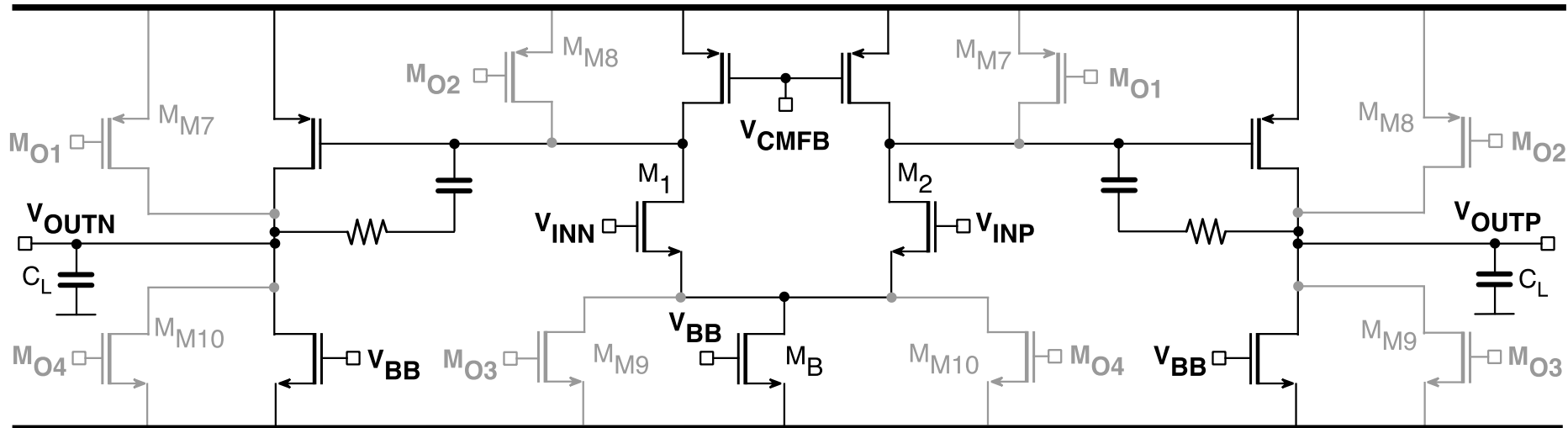
Generate $|I_1 - I_2|$ and increase the current in the differential stage by $k|I_1 - I_2|$. Positive feedback with a "fading" k



6.1 Low Voltage Low Power Analog Cells



Slew-rate monitor

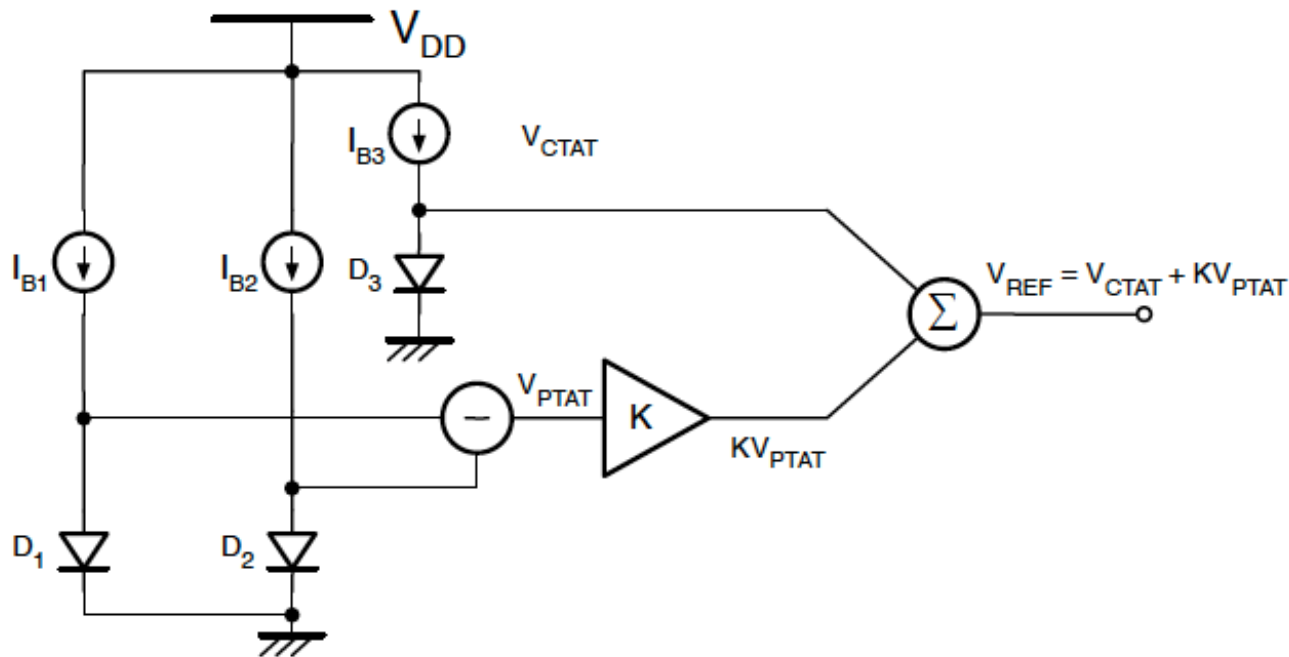


Op-amp With current boosting

6.2 Low Voltage Reference Generator

BAND GAP VOLTAGE REFERENCE

Needed to generate a temperature independent reference voltage



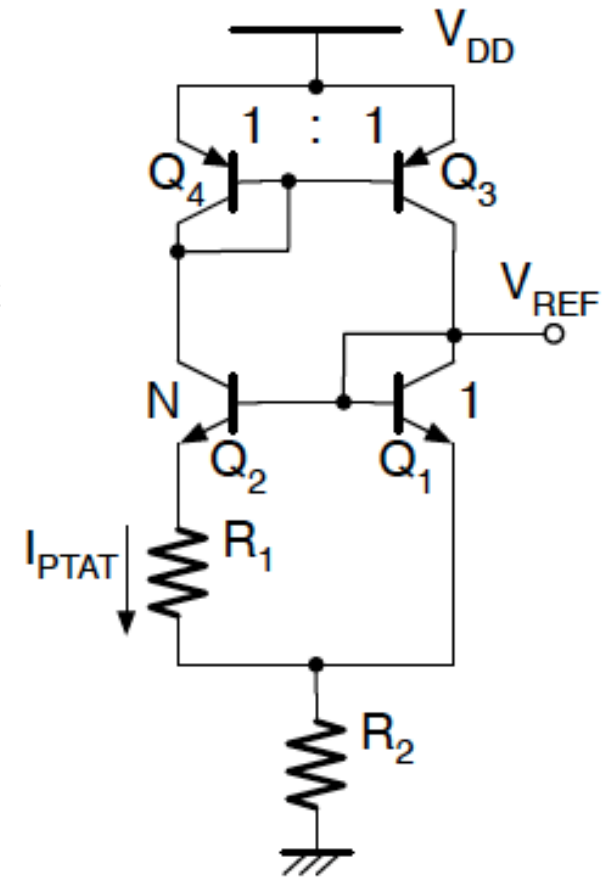
Use two “ingredients” with positive and negative T_C

V_{BE} negative T_C

V_T positive T_C

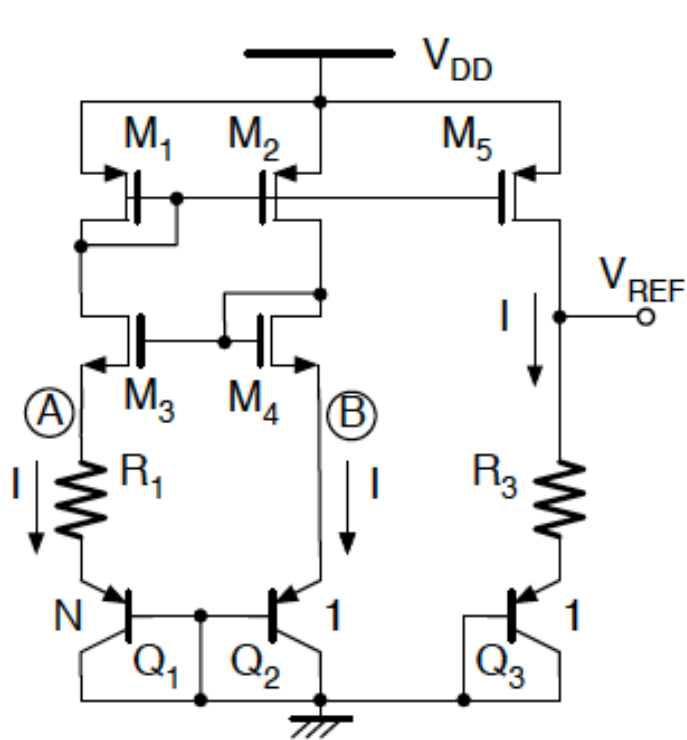
$$\Delta V_{BE} = \alpha V_T$$

$$i_C = I_S \left[\exp \left(\frac{V_{BE}}{V_T} \right) \right]$$

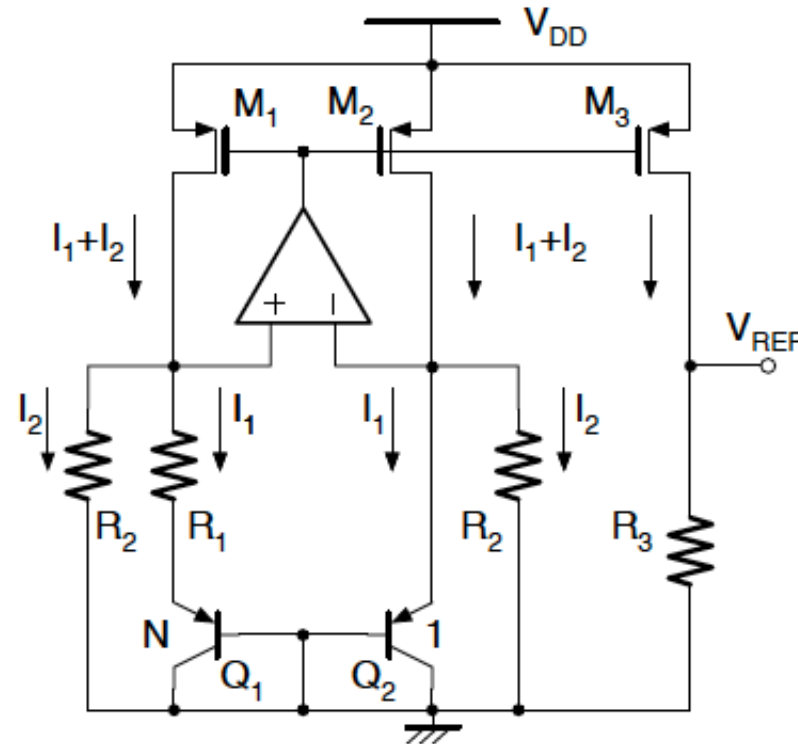


6.2 Low Voltage Reference Generator

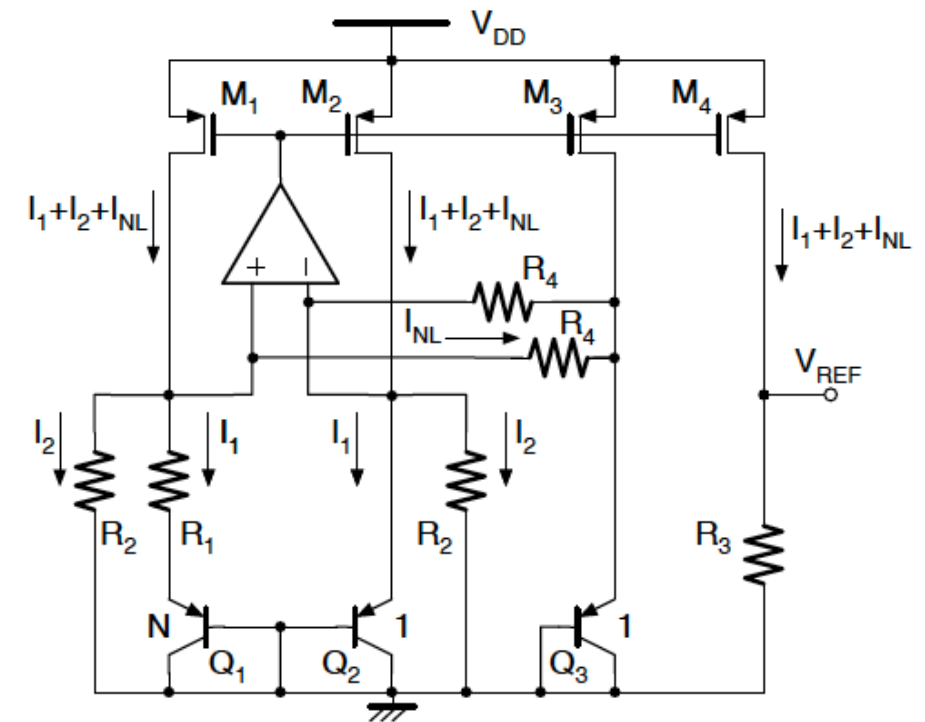
BAND GAP IMPLEMENTATIONS



Conventional



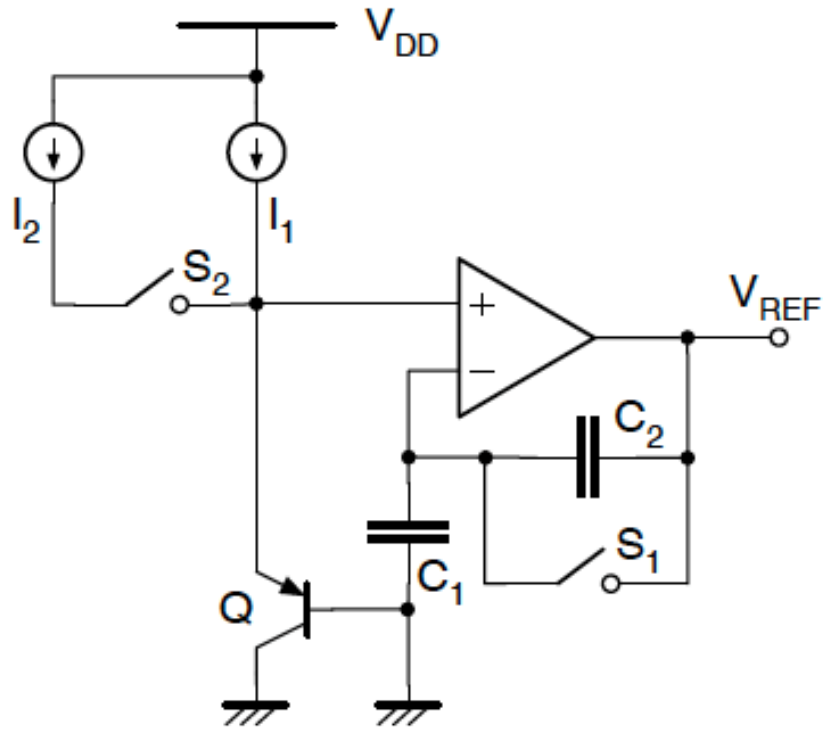
Banba



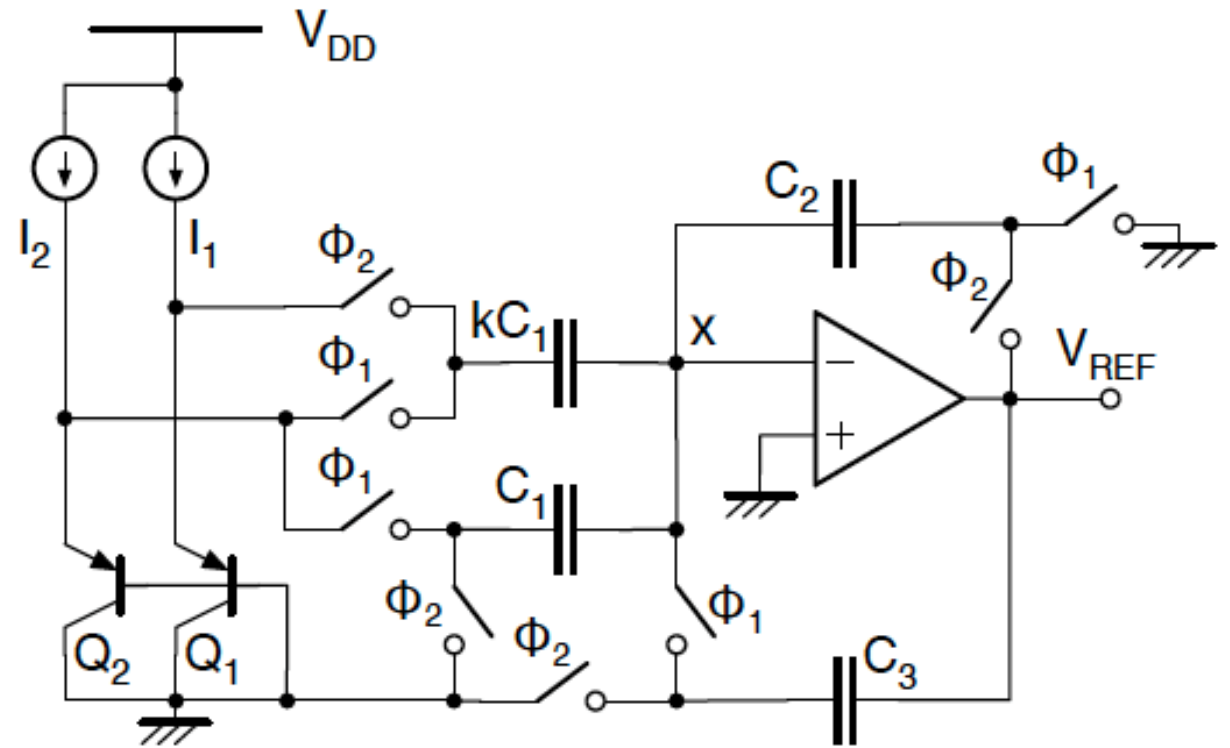
Malcovati, Pruzzi, Maloberti

6.2 Low Voltage Reference Generator

SC BANDGAP IMPLEMENTATIONS



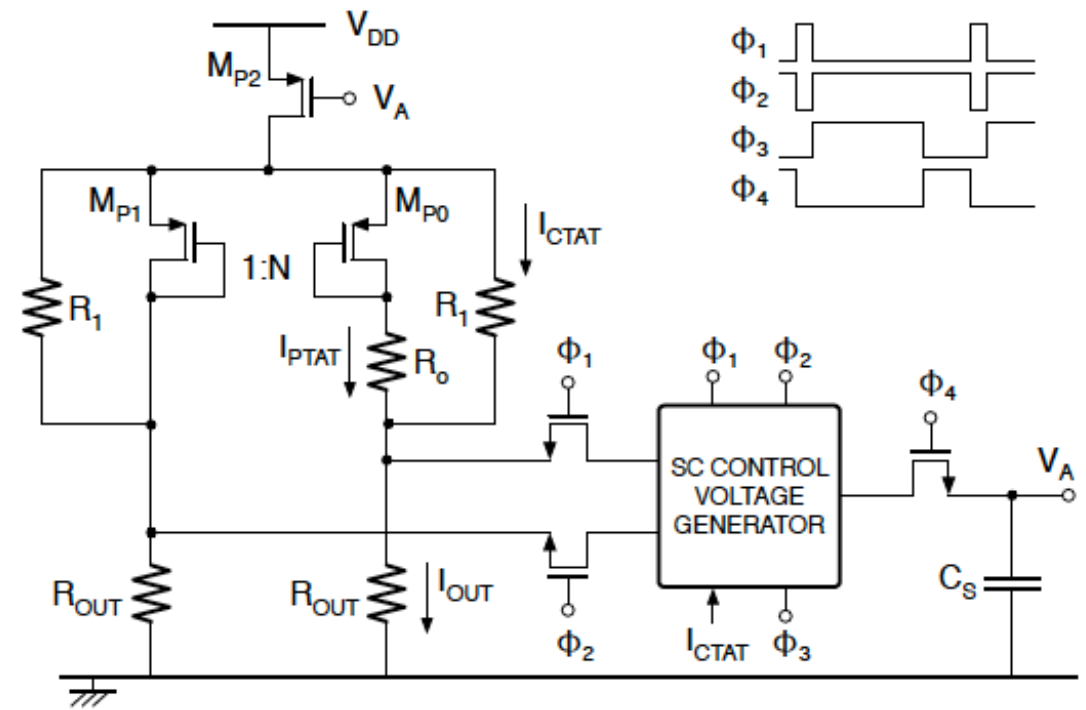
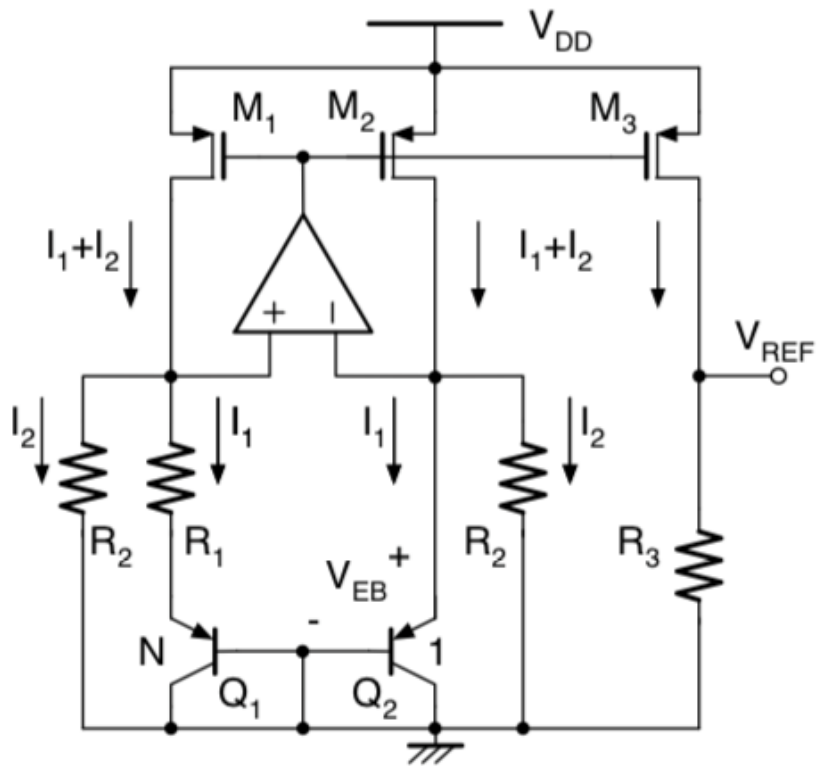
Gilbert, Shu



Jones, Martin (J-Wiley)

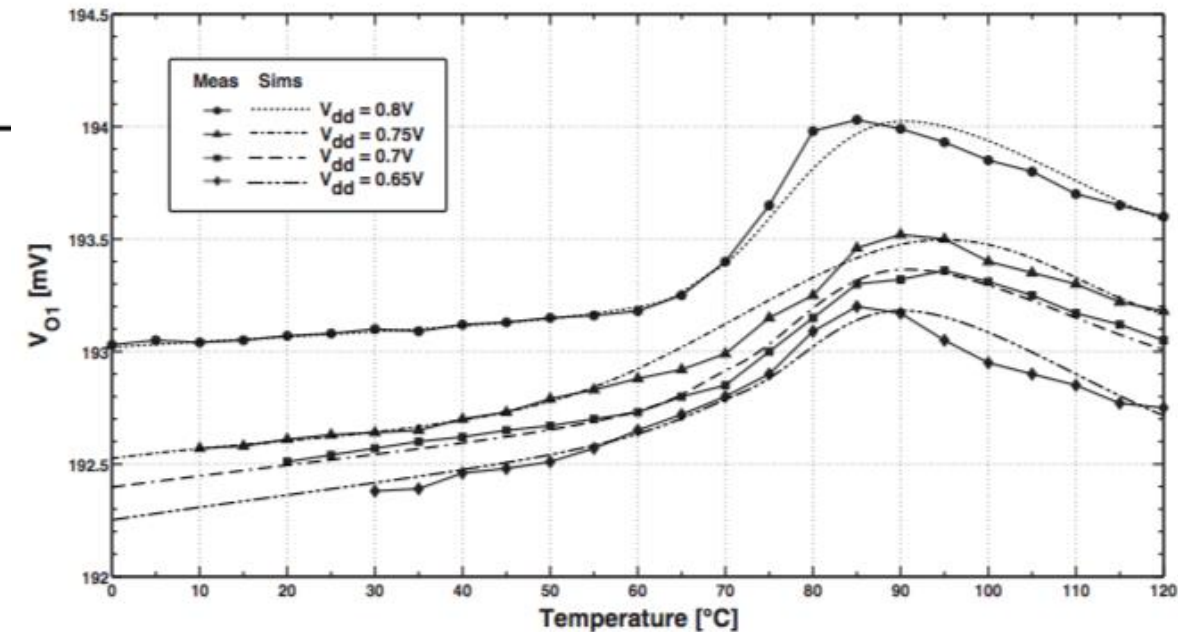
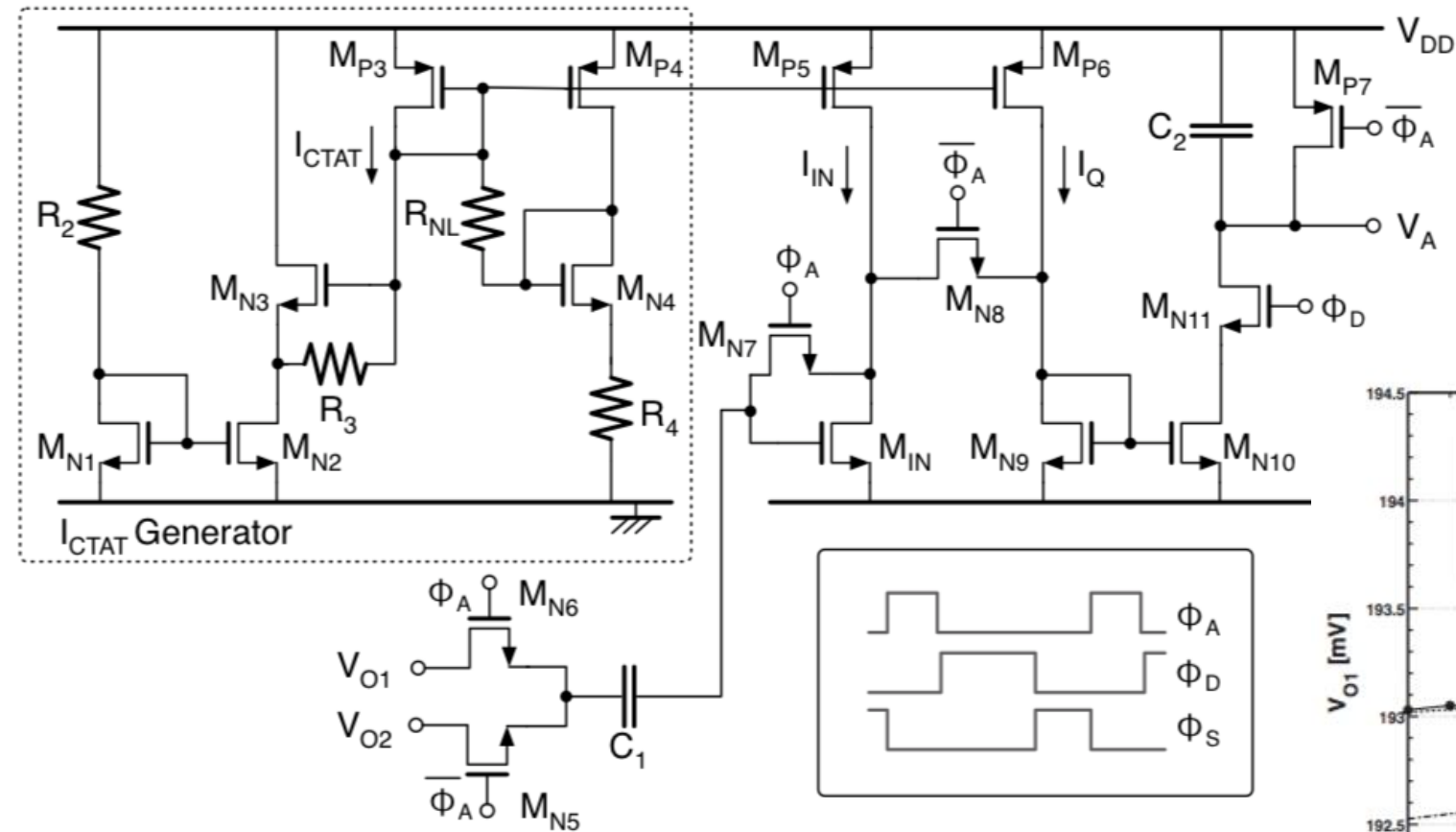
6.2 Low Voltage Reference Generator

ULTRA LOW-VOLTAGE BANDGAP (1)



P.B. Basyurt, D.Y. Aksin, E. Bonizzoni, F. Maloberti, "A 490-nA, 43-ppm/°C, sub-0.8-V supply voltage reference", IEEE European Solid-State Circuits Conference (ESSCIRC), pp. 115-118, 2014.

6.2 Low Voltage Reference Generator



6.2 Low Voltage Reference Generator

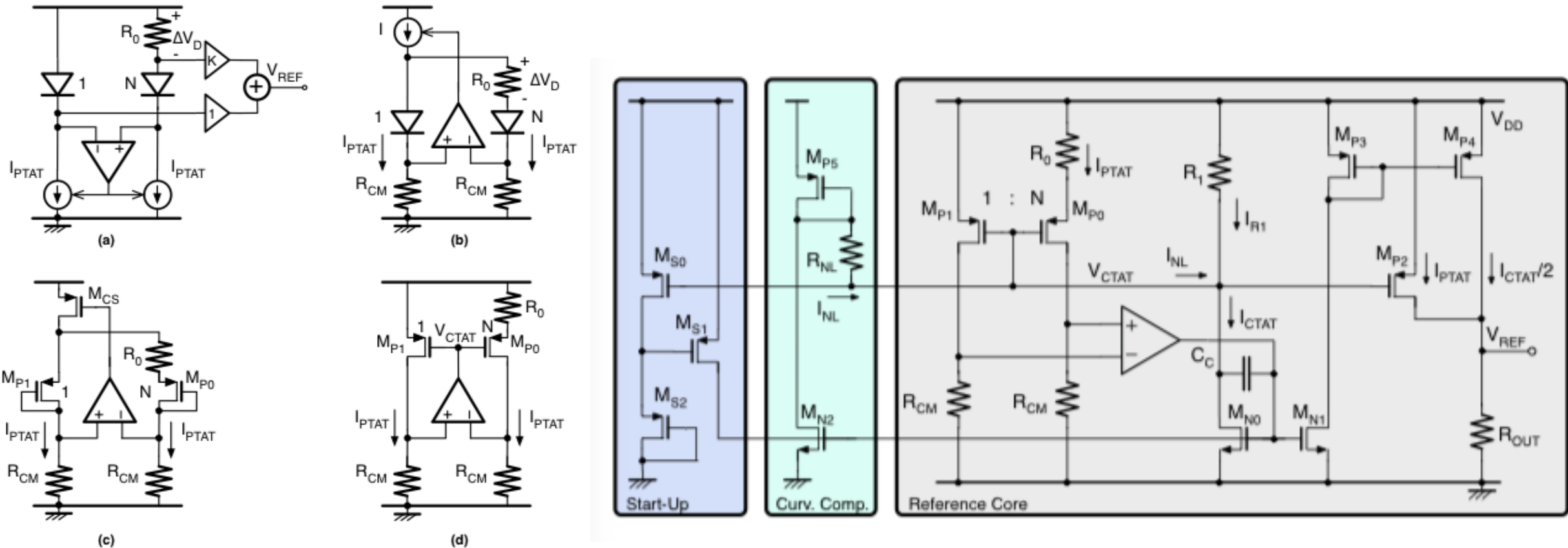
TABLE I. PERFORMANCE COMPARISON WITH SUB-1V BANDGAP REFERENCES IMPLEMENTED IN STANDARD CMOS TECHNOLOGIES.

	This work	[5]	[7]	[8]	[9]
Technology [μm]	0.18	0.13	0.18	0.6	0.35
Ref. Voltage [mV]	193	256	221	603	190.1
Min. Supply Voltage [V]	0.65	0.75	0.85	0.98	1
Sup. Current [μA]	0.49	0.2	3.9	18	0.25
TC [ppm/ $^{\circ}\text{C}$]	43	40	194	15	16.9
Temperature Range [$^{\circ}\text{C}$]	0-120	-25-85	-20-120	0-100	-40-80
PSR @ 100Hz [dB]	-50	N/A	N/A	-44	-41
PSR @ 10MHz [dB]	-36	N/A	N/A	-17	-17
Untrimmed Accuracy (3σ) [%]	0.8	3	N/A	N/A	N/A
Area [mm^2]	0.195	0.07	0.0228	0.24	0.049

- [5] V. Ivanov, R. Brederlow, and J. Gerber, "An Ultra Low Power Bandgap Operational at Supply from 0.75 V", *IEEE Journal of Solid-State Circuits*, vol. 47, no. 7, pp. 1515-1523, July 2012.
- [6] G. A. Rincon-Mora, "Voltage References: from Diodes to Precision Higher-Order Bandgap Circuits", New York: Wiley-IEEE, 2001.
- [7] P. H. Huang, H. Lin, and Y. T. Lin, "A Simple Subthreshold CMOS Voltage Reference Circuit with Channel Length Modulation Compensation", *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 53, no. 9, pp. 882-885, Sep. 2006.
- [8] K. N. Leung and P. K. T Mok, "A Sub-1-V 15-ppm/ $^{\circ}\text{C}$ CMOS Bandgap Voltage Reference without Requiring Low Threshold Voltage Device", *IEEE Journal of Solid-State Circuits*, vol. 37, no. 4, pp. 526-530, Apr. 2002.
- [9] H. W. Huang, C. Y. Hsieh, K. H. Chen and S. Y. Kuo, "A 1V 16.9ppm/ $^{\circ}\text{C}$ 250nA Switched-Capacitor CMOS Voltage Reference", *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp. 438-440, Feb. 2008.

6.2 Low Voltage Reference Generator

ULTRA LOW-VOLTAGE BANDGAP (2)



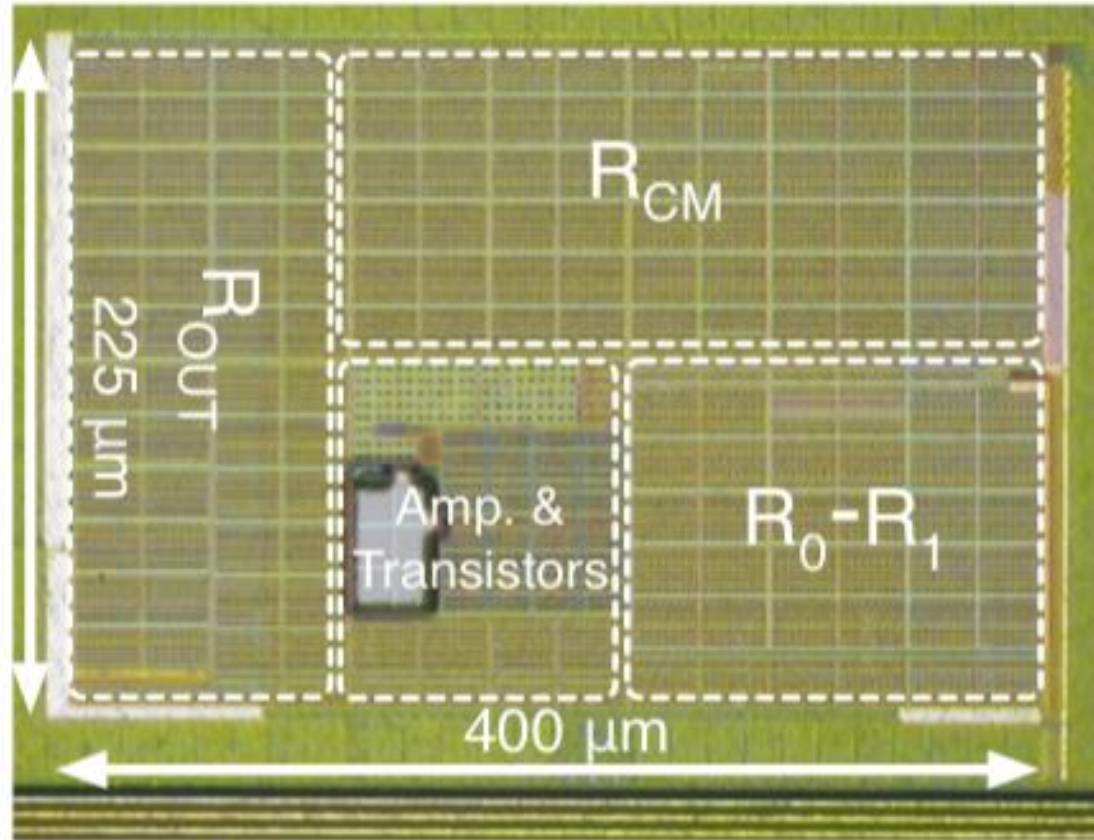
P.B. Basyurt, E. Bonizzoni, D. Aksin, and F. Maloberti, "A 0.4-V Supply Curvature Corrected Reference Generator with 84.5 ppm/ $^{\circ}$ C Average Temperature Coefficient within -40 to 130 $^{\circ}$ C", IEEE TCAS II - 2016

6.2 Low Voltage Reference Generator

TABLE I. PERFORMANCE SUMMARY AND COMPARISON WITH OTHER PUBLISHED STATE-OF-THE-ART REFERENCE CIRCUITS.

Parameter	This Work	[8]	[10]	[12]	[11]	[13]	[9]	[14]
CMOS Technology [μm]	0.18	0.18	0.13	0.09	0.18	0.18	0.13	0.18
Output Voltage [mV]	212.4	257.5	500	241	193	548	185	323
Minimum Supply Voltage [V]	0.4	0.45	0.5	0.55	0.65	0.7	0.75	0.75
Power Consumption [nW]	192	2.6	32	482000	318.5	52.5	170	4000
TC [ppm/ $^{\circ}\text{C}$]	84.5	165	75	150	43	114	40	15
Temperature Range [$^{\circ}\text{C}$]	-40–130	0–125	0–80	10–100	0–120	-40–120	-20–85	-60–130
PSR @100Hz [dB]	-40	-45	-40	-35	-50	-56	N/A	-34 _a
Untrimmed Accuracy (3σ) [%]	2 ^b	12	2 ^b	5	0.8	4.8	3	N/A
Area [mm^2]	0.09	0.043	0.0265	0.07	0.195	0.025	0.07	0.039

6.2 Low Voltage Reference Generator



- [8] L. Magnelli, F. Crupi, P. Corsonello, C. Pace, and G. Iannaccone, "A 2.6nW, 0.45 V Temperature Compensated Subthreshold CMOS Voltage Reference", *IEEE Journal of Solid-State Circuits*, vol. 46, no. 2, pp. 465–474, Feb. 2011.
- [9] V. Ivanov, R. Brederlow, and J. Gerber, "An Ultra Low Power Bandgap Operational at Supply from 0.75 V", *IEEE Journal of Solid-State Circuits*, vol. 47, no. 7, pp. 1515–1523, July 2012.
- [10] A. Shrivastava, K. Craig, N. E. Roberts, D. D. Wentzloff, and B. H. Calhoun, "A 32 nW Bandgap Reference Voltage Operational from 0.5 V Supply for Ultra-Low Power Systems", *IEEE Solid-State Circuits Conference Dig. Tech. Pap.*, pp. 94–95, Feb. 2015.
- [11] P. B. Basyurt, E. Bonizzoni, D. Y. Aksin, F. Maloberti "Voltage Reference Architectures for Low-Supply-Voltage Low-Power Applications", *Microelectronics Journal*, vol. 46, no. 11, pp. 1012–1019, Nov. 2015.
- [12] P. Kinget, C. Vezyrtzis, E. Chiang, B. Hung, and T. L. Li, "Voltage References for Ultra-Low Supply Voltages", *Proc. of IEEE Custom Integrated Circuits Conference*, pp. 715–720, Sept. 2008.
- [13] Y. Osaki, T. Hirose, N. Kuroki, and M. Numa, "1.2-V Supply, 100-nW, 1.09-V Bandgap and 0.7-V Supply, 52.5-nW, 0.55-V Subbandgap Reference Circuits for Nanowatt CMOS LSIs", *IEEE Journal of Solid-State Circuits*, vol. 48, no. 6, pp. 1530–1538, June 2013.
- [14] C. M. Andreou, J. Georgiou, "A 0.75-V, 4- μ W, 190°C Temperature Range, Voltage Reference", *International Journal of Circuit Theory and Applications*, Aug. 2015. DOI: 10.1002/cta.2122

**The World of ~~Analog~~
Micropower**



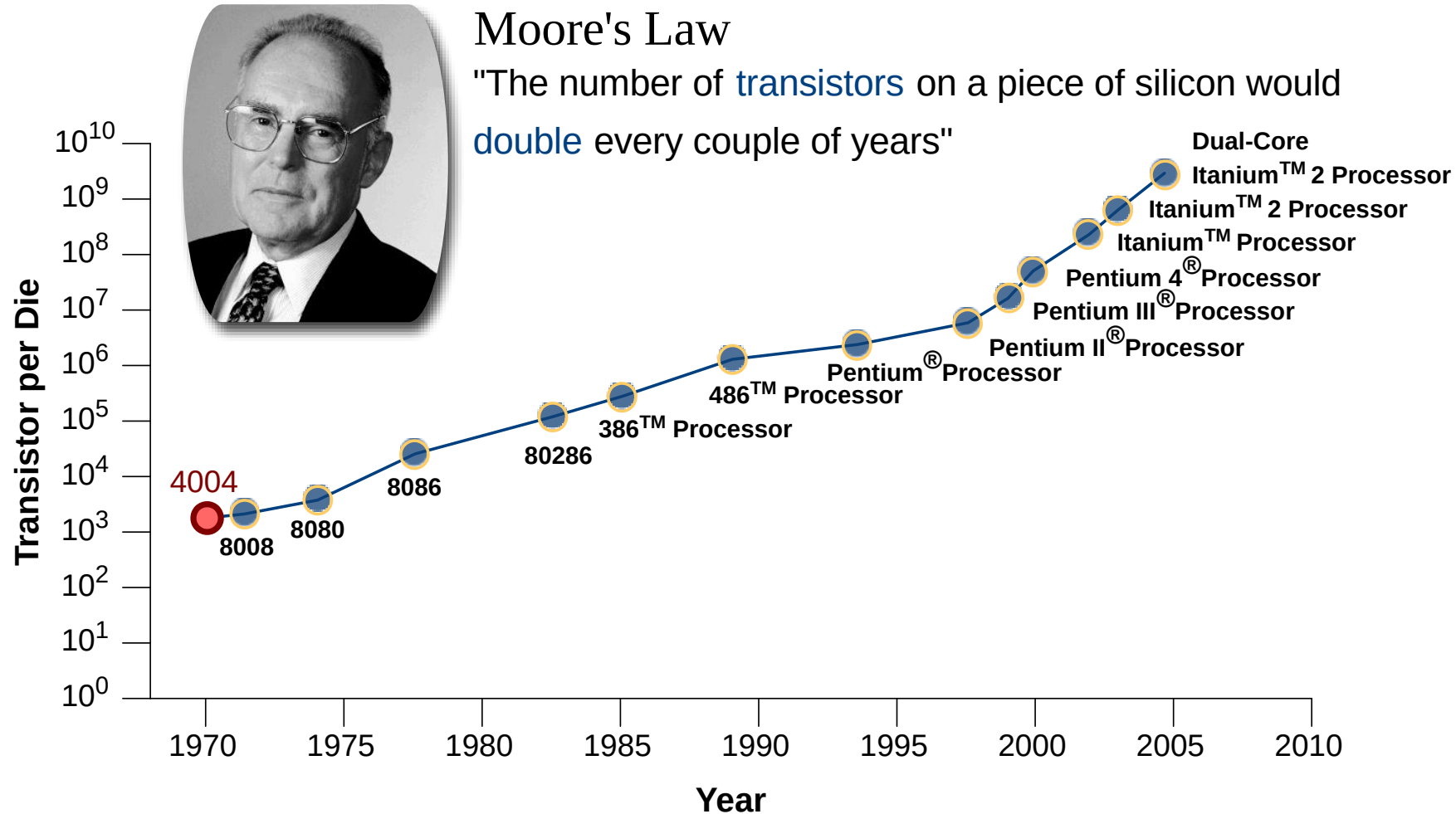
**The World of Systems
with micro-power consumption**

MULTIDISCIPLINARITY

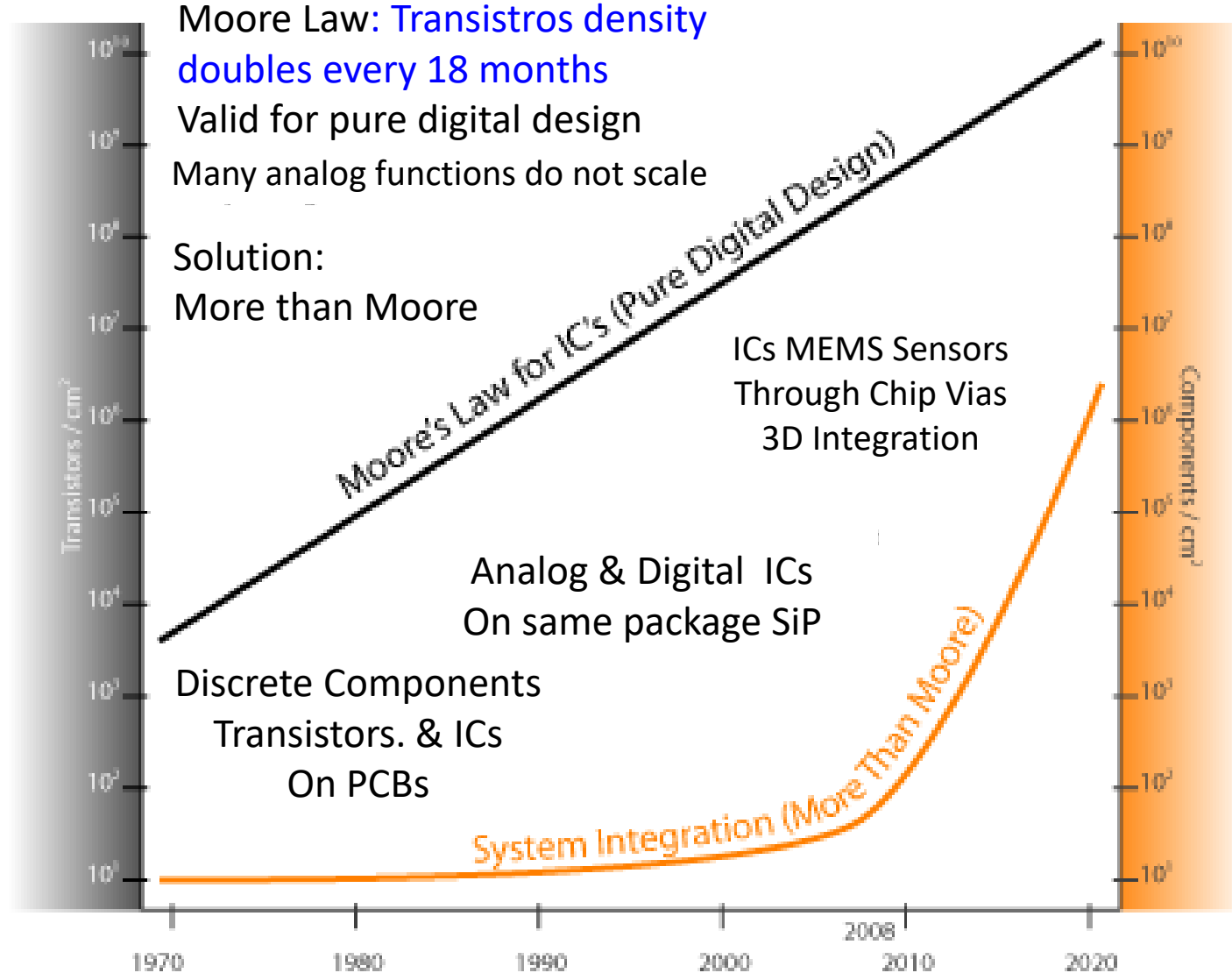
System matters ... then, single function are not so important

Conclusions

The microprocessor(μp)

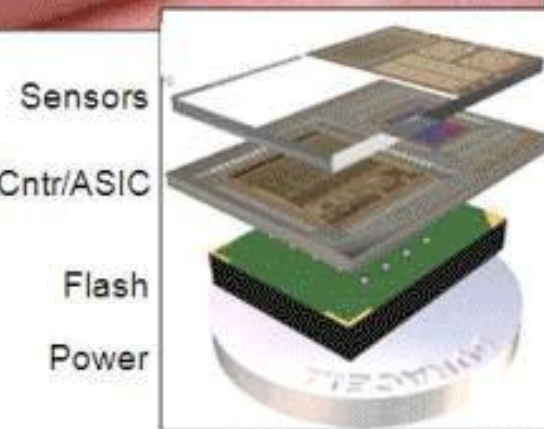
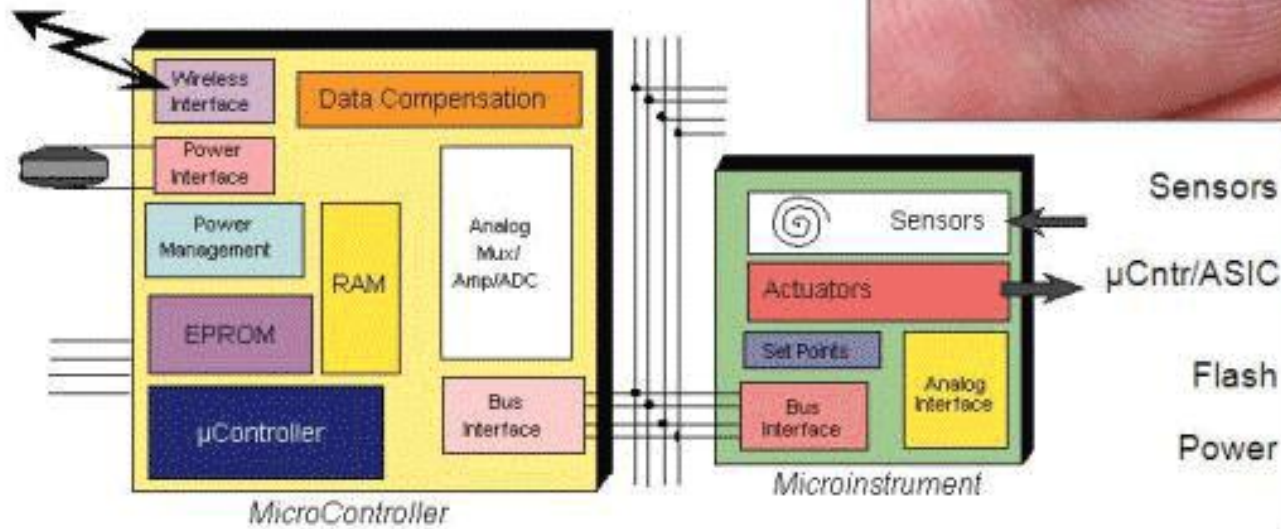
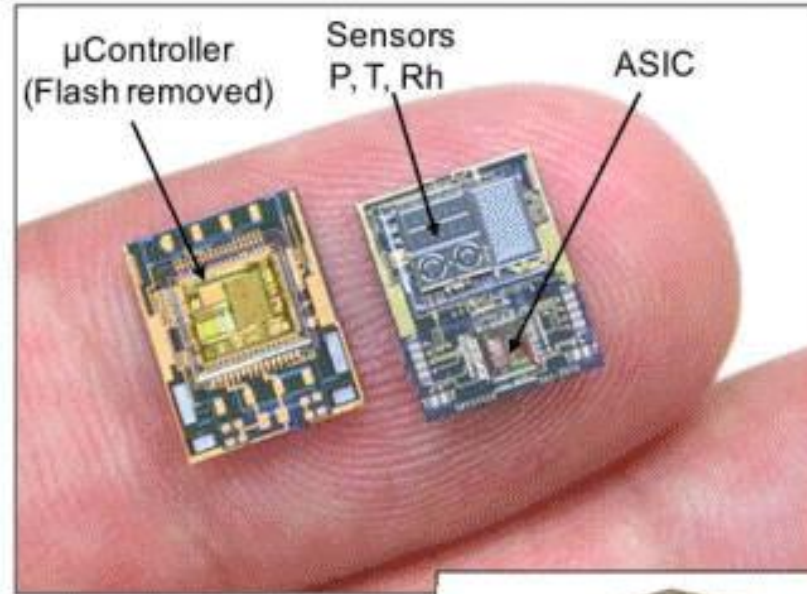
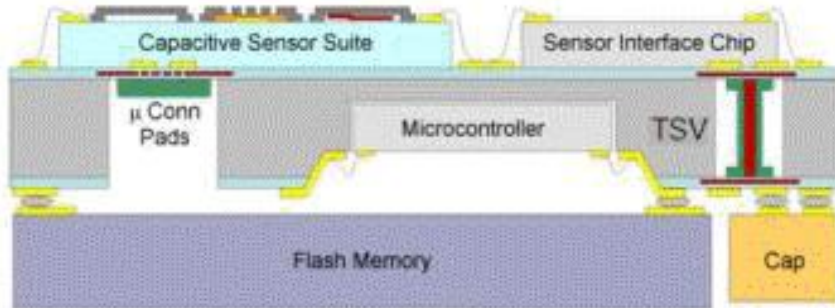


Conclusions

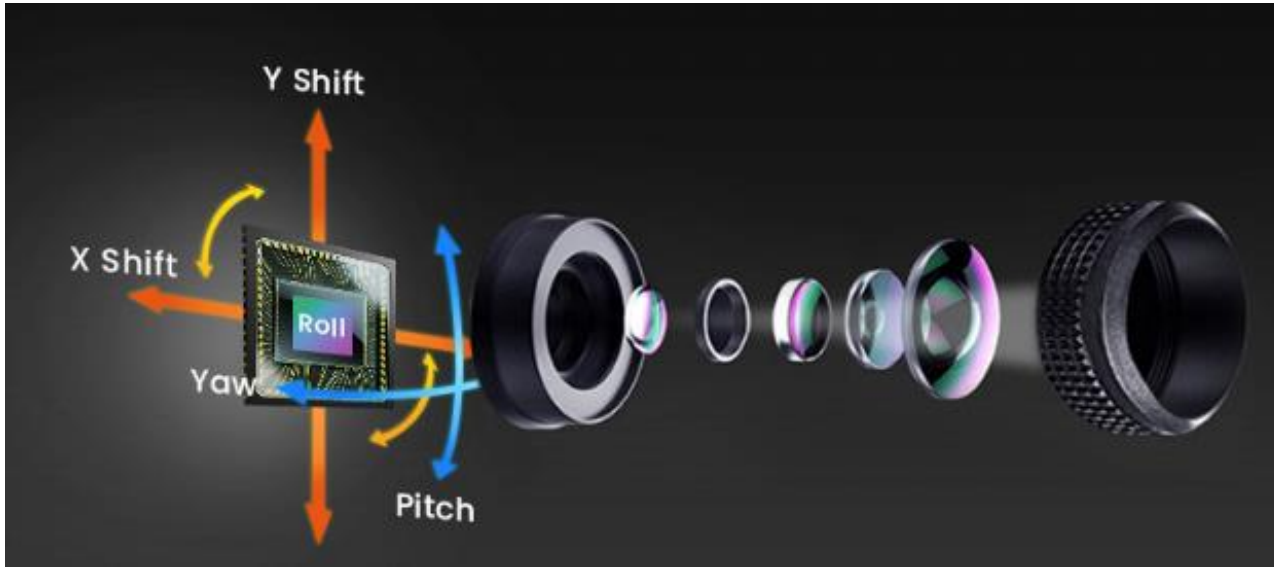


Conclusions

Moore than Moore is pushing technology in a “different” direction



Conclusions



Don't just focus on deep submicron technologies, other technologies and method can be disruptive (and rewarding)

